Efficient Power Conversion's DC-DC Converter Handbook: Power Architectures

Steve Taranovich - November 02, 2015

Editor’s note: I had previously reviewed this book by Efficient Power Conversion's talented power experts and found it to be very instructive for power designers, students, and anyone interested in learning how to design a DC/DC converter-based power supply using GaN power transistor elements. Here I bring you Chapter 1 and I will follow with Chapters 2, 3, and 4. See my review of this book [here](#).

Overview of power architectures

Introduction

The advent of commercial and cost-effective gallium nitride (GaN) power transistors heralds a new age in power electronics [1]. The intent of this handbook is to aid in the adoption of GaN power transistors by examining power solutions for data centers and telecommunications systems through hardware examples. This handbook examines the benefits of enhancement-mode gallium nitride FETs (eGaN FETs) in power conversion applications with an input voltage range centered around 48 VDC with load voltage as low as 1 VDC.

Data centers and telecommunication systems are a key part of the nervous system of the electronic infrastructure that supports a large part of daily human activities. The technology is so integrated into daily life that it has become taken for granted, but like an iceberg, the majority of this infrastructure is hidden from view. The hardware of this infrastructure is comprised of millions of microprocessors, data storage, information buses, and ancillary logic.

Each processor can have billions of microscopic integrated transistors [2]. These tiny devices consume minuscule amounts of power, and generally operate near one volt or even less. However, a data center can have many thousands of processors, which means trillions of transistors are in use at any given moment [3]. This translates into data center power requirements from a few megawatts to tens of megawatts. In practice, the latter nominally requires 3-phase 4160 VAC or 13.8 kVAC from the utility. This is completely unsuitable for information processing hardware, hence there is a great deal of thought and attention towards power architectures and power conversion technologies to get from these high input voltages down to just one volt.
Why is this so important?

The first answer is that electricity costs money, and data centers use a lot of electricity. There are several levels of power conversion to accomplish greater than the 1000:1 voltage conversion ratio required, and each one loses some energy in the conversion process and contributes to the overall system cost. The lost energy is in the form of heat, which must be removed. This usually requires active thermal management, which in turn requires even more electricity, occupies valuable space, and adds even more cost. Efficient power conversion lowers one of the largest contributors to data center operating cost - the electricity bill.

Second, the power conversion hardware takes space, and some of that space is on the motherboards that process information. Information processing makes money, and power conversion costs money, so it is in the interest of data centers’ owners to maximize the former and minimize the latter.

Finally, the energy used by data centers is becoming a significant fraction of total energy usage [4]. Minimization of energy usage and waste has a significant environmental benefit.

Why low voltage power?

Why low voltage power?

What is the motivation for a focus on lower voltage power? There are two main reasons. First, at the lowest voltage, the power conversion directly touches the information processing. This forces a stringent set of performance requirements on the power electronics that is particularly challenging, especially on size, power density, and transient response. The second reason is that most of the conversion loss is at low voltage, and the lower voltage goes, the worse it gets. This is shown in Figure 1.1.
Losses at the low voltage stages of the system dominate the overall losses. At higher voltage and power, higher efficiencies are already common, so there is less room for improvement. Thus, while advanced technology may reduce cost or improve power density at the high-voltage and high-power part of the system, there are limited energy savings to be had. On the other hand, advances at the low voltage end can have large benefits for power density, cost, and efficiency. Increased low-voltage efficiency propagates all the way through the system, reducing power requirements for the upstream power components and their associated loss and cost.

Table 1.1 provides some numerical evidence. Consider the system of Figure 1.1 as our baseline, with a total load power of 1 MW. For Case 1, we improve the high-voltage power electronics, namely the UPS and the rectifiers, by cutting the relative loss in half. This cuts the total data center losses by 45 kW, or 17%. For Case 2, the losses of the intermediate bus converter (IBC) and the Point-of-Load (POL) converter are cut in half, for a savings of 98 kW - more than 36%! Thus, improvements in the two lowest voltage stages have far more impact than from improvements in the three upstream stages of higher voltage converters.
final load power of 1 MW. Case 1 cuts relative losses of higher voltage power electronics by half, and Case 2 does the same for the low voltage power electronics. Improved efficiencies are shaded for each case, and the bottom line shows the effect on overall system performance.

eGaN FETs show large benefits in the low-voltage parts of the system, and goal of this book is to show how to obtain this benefit by giving specific hardware examples. The remainder of this chapter is devoted to a review of low voltage power architectures for telecommunication and data center applications. The evolution of these architectures, which are typical architectures in common use today, as well as possible paths for the future will be discussed.

Low voltage power architectures

In this section, a brief overview of different low voltage power architectures will be given. A good reference for this discussion is material from the Texas Instruments’ seminar, “Improving System Efficiency with a New Intermediate-Bus Architecture” [10], as it provides an in-depth discussion as well as an extensive bibliography for those wishing to delve deeper into the subject.

Rack level power

A server cabinet, or rack, contains a large number of blades or slices, each of which is comprised of a motherboard with CPUs, RAM, additional logic, and disk storage. In a typical setup, AC power is delivered to the rack, where at some point it is converted to the multiple DC voltages required for data processing. A high-level view of how this power conversion is accomplished is referred to as the rack or cabinet power architecture. For this discussion, only the rack power architecture, which we refer to as the “power architecture” for brevity, is of concern. A typical rack is shown in Figure 1.2 [11], with power consumption ranging from about 8 kW to more than 20 kW [12].
The power architecture has a wide range of possibilities, but in practice these can be classified in a relatively small number of groups. There is always some overlap between groups, and therefore these groups should be considered as general guidelines.

The key power architecture requirements are:

- Power density
- Efficiency
- Availability (Up-time)
- Cost
- Ease of design
- Safety

The first requirement, high power density, is desirable for two main reasons. First, the large current transients from microprocessors require that power conversion takes place physically adjacent to the microprocessor in order to minimize voltage drops due to bus impedance. However, the space near the microprocessor is constrained due to the need for high-speed data buses to memory and
I/O, and the need for thermal management of the microprocessor itself. Secondly, the purpose of the server is information processing. Power conversion electronics are considered a cost, whereas information processing provides the revenue. If you can reduce the total area of the motherboard devoted to power conversion, the area saved by doing so can now be devoted to information processing.

Efficiency is a second key requirement. Efficiency has a direct impact on operating cost, while at the same time it has a number of indirect effects that have a large net impact on the system. Power loss is the dominant indirect effect. It shows up as heat, and heat must be removed to maintain reliability and to prevent further decreases in efficiency. Thermal management adds to three costs – energy cost, material cost, and design cost. Finally, increases in power density require increases in efficiency to keep heat flux at a manageable level.

The third requirement of availability is related to reliability. Downtime is costly, and the ability to allow design considerations like redundancy and hot-swap capability reduces downtime. Such capabilities require increasingly sophisticated controls and power conversion topologies that can control power effectively under a variety of conditions.

The fourth requirement is cost. Cost must be kept under control. No one wins if data centers lose money.

The fifth requirement is ease of design. Data centers are complex entities that require a great deal of design effort. The adoption of standards, combined with flexible and sophisticated power converters, can make a significant contribution to reducing design time and cost.

The final requirement is safe operation – for both people and equipment. In addition to minimization of failures that endangers people and equipment during normal operation, systems must be designed not only to fail in a safe manner, but also have the capability to be repaired in a safe manner while the data center remains operational.

The power architecture design task is a complex optimization problem that requires balancing all six requirements. This balancing shapes the power architecture and results in a cascade of further requirements that flows down to the level of individual components. However, these lower-level requirements cannot always be met with the technologies at hand, so component level technologies have a fundamental impact on system architecture. As component technologies evolve, so do the systems. The remaining chapters will show that eGaN FETs provide large improvements in power supply technology. In addition to discussing how they will greatly benefit existing power architectures, the possibilities of how they can enable future architectures will be examined.
Centralized power architectures were developed when the telecom industry moved from electromechanical switchgear to electronic switching systems. Figure 1.3 shows a simplified centralized power architecture diagram. The electronic switching system ran on a minus 48 V Vin DC bus that was supplied by massive banks of lead-acid batteries (not shown). Since the batteries provided an extremely reliable power source, this concept has endured. The batteries were normally charged from a rectifier (AC/DC converter). The main DC bus used switching converters to provide multiple low voltage buses on a backplane, which fed an array of cards that did the data processing.

This system required a massive and expensive backplane to carry multiple voltages, some at high currents, while minimizing voltage drops. Since the power supply is a single point of failure, the DC-DC converter was heavily overdesigned, contributing to a long design time. The complexity, and extended downtime that follows complexity, made it expensive to maintain. The power system was expensive to upgrade as well, and this limited the ability to take advantage of advances in data processing technology. However, this centralized architecture represented state-of-the-art power technology for many years.
Today, this architecture is used in legacy systems that are gradually being replaced with modern systems; hence, it is disappearing.

**Distributed power architecture (DPA)**

As switch-mode power conversion advanced and costs came down, it became practical to supply each card with its own multi-output DC-DC converter, resulting in the distributed power architecture (DPA), as shown in **Figure 1.4**. The DPA enabled the use of a single minus 48 VDC backplane power bus and the use of higher voltage meant much lower currents and much less copper in the backplane bus. The regulation at the card level meant that the backplane bus did not need to be tightly regulated. These two features greatly reduced complexity and cost. Furthermore, the system availability was greatly enhanced since it removed a single point of failure. An added bonus was that the isolation at the card level resulted in improved EMI (both generated and received), as well as removing a path for circulating ground currents that could raise system noise levels, and in some cases cause dangerous faults.

![Figure 1.4: Distributed Power Architecture (DPA)](image)

The cost of DPA systems was still high. The DC-DC converters remained as custom designs, limiting the ability to take advantage of advances in data processing technology. In particular, the trend towards lower voltages for the digital hardware caused increasing pain to the designers for both the converters and interconnects. Power converter technology continued to advance, especially with the
maturity of the power MOSFET and the development of an extensive portfolio of power management integrated circuits (ICs). This led to the next advance in power architecture, the intermediate bus architecture (IBA). Thus, the DPA, as shown, is “not recommended for new designs.”

Intermediate bus architecture (IBA)

The IBA, as shown in Figure 1.5, is the natural extension of the DPA. Advances in power electronics resulted in large improvements in power density, efficiency, and cost. In addition, standards, known as the Distributed-power Open Standards Alliance (DOSA) standards [13], evolved for power converter blocks based on available “brick” converters.

Around the same time, CPU voltages had dropped below 2 V. CPU power dissipation became so high that the startup and shutdown of CPU subsystems was required to help manage temperatures. This resulted in very large and fast current transients in the CPU power bus, which with the ever-decreasing bus voltage, required that power converters be physically adjacent to the CPU. These converters, known as voltage regulator modules (VRMs), also helped drive the acceptance of self-contained point-of-load power converters (POLs).
These developments enabled placement of the majority of the DC-DC switch-mode power conversion directly on the motherboards. A DC bus, based loosely on the 48 V bus used in prior systems, goes directly to the motherboards. These boards contain one or more intermediate bus converters, which provide an intermediate bus voltage of nominally 12 V on the motherboard. This intermediate bus is then converted with a POL converter at, or near, each critical load.

This system adds a number of benefits to the original DPA. The bus voltages are flexible and can be optimized by the power architect to benefit the overall system. Furthermore, system upgrades are greatly simplified, since most of the power processing is on the blades that would be replaced during an upgrade. As the IBA has become widely adopted, intermediate bus converters (IBCs) and POLs have become more advanced, not only in terms of raw performance, but also in features, including digital control, monitoring and diagnostics.

The benefits of the IBA (see Figure 1.6) have resulted in its wide adoption. While there is debate about the best voltages, paralleling, isolation and regulation, the IBA is the most widely accepted architecture today. The benefits of the IBA are summarized below:

- Reduced backplane bus costs
- Higher efficiency
- Reduced design time
- Isolation between blades or motherboards
- Higher availability
- Greater flexibility

**Details of IBA**

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The IBA is a highly flexible architecture, so a designer has many decisions to make, bounded by the needs of the design and the features of the available IBCs and POLs. The basic choices are:
Backplane voltage

The typical telecom backplane voltage could vary over a range of 36–75 V, in part because a battery was present directly on the bus and the battery voltage could vary with state of charge, load, temperature, age and charging current. With the increasing adoption of switch-mode rectifiers and high power UPS battery-bus interfaces, it is now possible to better regulate the bus. This has allowed the development of converters with a narrower system bus voltage range in exchange for the higher efficiency of the IBC. In our examples, we assume a nominal bus voltage of 50 V, with the understanding that some variations will be present.

Intermediate bus voltage

The intermediate bus voltage is the voltage on the motherboard power planes. A higher voltage means less loss on the plane and in connections to and from the plane, but requires a larger conversion ratio for the POLs. The higher intermediate bus voltage results in lower efficiency for the POL converter [10], which may cause problems with thermal management. The physical proximity of the POL converter to the power-dissipating load makes this problem worse.

Regulated or unregulated intermediate bus

The regulation provided by the POL converters means that a regulated intermediate bus is not
strictly necessary. The primary advantage of an unregulated intermediate bus is that the IBC can be optimized for efficiency by operating as close to 100% duty cycle as possible. When operating at a very high duty cycle, the output filter inductance is also significantly reduced, enabling higher power density and minimizing inductor resistance. In the case of an unregulated intermediate bus, the IBC acts as a DC transformer (DCX) [14]. This means that any variation in the system bus voltage appears on the intermediate bus. This may be tolerable, but may make optimization of the POL converters difficult.

A regulated IBC will usually have a lower efficiency than a comparable unregulated IBC. For a given power, the larger range of duty cycle results in higher RMS currents throughout the converter and also forces the use of a larger inductor with higher resistance to accommodate the increase in volt-seconds. The regulation of the intermediate bus voltage has a number of benefits. A wider system bus voltage variation is possible without impacting the efficiency of the subsequent POL converter. The intermediate bus voltage can also be adjusted to optimize the overall system efficiency by reducing the bus voltage to gain efficiency benefits in the downstream POL converters. The additional control capability required for regulation can also be used to implement additional features, including droop control for paralleling, dynamic optimization, and system monitoring and diagnostics.

**Location of isolation**

Finally, safety and fault tolerance almost always result in a requirement for galvanic isolation.

Today, transformers are the only practical means of providing isolation. While this isolation can be provided at the cabinet level in the AC-DC converter, it is highly desirable to provide isolation at the motherboard level. In addition to safety, this isolation can reduce EMI, including the prevention of large, low frequency ground currents from flowing between the cards in a rack.

The use of a transformer in a power converter comes with significant efficiency, power density, and cost penalties. These are mitigated to a certain extent by the benefit provided by the transformer turns ratio, but in general the former outweighs the latter, especially at lower voltages and higher currents. As a result, there has been significant recent consideration of non-isolated IBAs.

A listing of the general properties of the IBA and the POL power conversion system architectures is given in **Table 1.2**: 
## Table 1.2: Summary of general properties of IBCs and POLs

<table>
<thead>
<tr>
<th>Intermediate Bus Converter (IBC)</th>
<th>Point-of-Load Converter (POL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Transformer-isolated</td>
<td>• Non-isolated</td>
</tr>
<tr>
<td>• Standard footprint</td>
<td>• Standard and non-standard footprints</td>
</tr>
<tr>
<td>• Transformer turns ratio between 3:1 and 5:1</td>
<td>• Regulated</td>
</tr>
<tr>
<td>• May be regulated or unregulated</td>
<td>• Buck converter</td>
</tr>
<tr>
<td>• Several possible topologies</td>
<td>• Low output voltage: 0.9 to 3.3 V typical</td>
</tr>
<tr>
<td>• Increasing intelligence and control sophistication</td>
<td>• Output currents: 10s of amps</td>
</tr>
<tr>
<td>• Power levels of 100 W approaching 1 kW</td>
<td></td>
</tr>
<tr>
<td>• Input voltage ~48 V</td>
<td></td>
</tr>
<tr>
<td>• Output voltage 5 – 14 V</td>
<td></td>
</tr>
</tbody>
</table>

**DC Bus Architecture (DCBA)**

The last architecture to be considered, referred to in this book as DC Bus Architecture (DCBA), is not yet commonly used, but is the subject of considerable discussion due to the advent of superior semiconductors such as eGaN FETs. In the DCBA, as shown in figure 1.7, a high-voltage DC bus feeds the motherboards, as with the IBA. However, unlike the IBA, there is no intermediate bus converter. The DC bus is continued on the motherboard and POL converters are used to convert the system bus voltage directly to the load voltage. Note, this is normally discussed in the context of a 48 VDC bus, but there has been discussion of using voltages as high as 380VDC in this application [15].
One of the benefits of the DCBA is a low-current backplane, similar to the DPA and IBA, but with the potential for even lower current and losses. This would further enable low-current planes on the motherboard and reduce losses here as well. Another perceived benefit is higher efficiency due to the elimination of one or more power stages. In addition to efficiency, there is an apparent simplicity about the system, which often translates into cost and reliability benefits.

With silicon MOSFET technology, the efficiency gains are minimal. As discussed at the beginning of this chapter, most of the losses occur at the lowest voltage stage, but the DCBA eliminates the higher voltage stages, so the gains are small.

Before the claim of simplicity can be made, there are numerous unsolved problems that are in the way of adoption of this system. One of the key problems is isolation. Galvanic isolation may solve many systems problems; however, only transformers, which can have a large negative impact on power density and efficiency, currently provide practical and efficient isolation. One solution to this
problem may be the use of capacitive isolation, which becomes practical as one approaches VHF switching frequencies (30 MHz - 300 MHz), but VHF power conversion is in its infancy.

Another big problem is the effect of high-voltage on safety and reliability. For a 48 V system, the concerns are small, but as the bus voltage gets higher, new problems arise. As PCB geometries become smaller and interconnect density higher, the spacing between traces and layers gets smaller. Normally minor concerns like dielectric degradation and leakage, whisker growth, and migration of dielectric become bigger problems. At 380 VDC, these could be extremely challenging problems. Even outside the rack, 380 VDC has numerous unsolved problems, including DC breakers and arc flash protection [16].

eGaN FETs and the DCBA

GaN power semiconductors provide large improvements over silicon MOSFET performance, providing positive implications for the widespread adoption of DCBA. In chapter 6, it will be shown that eGaN FETs make it possible to design high-conversion-ratio POL converters with a 48 VDC input that have the potential to meet efficiency and power density requirements. At 48 V, the motherboard bus currents can be reduced by a factor of four, and losses by a factor of 16. Area now devoted to power conversion, may be repurposed to information processing.

Clearly, work is needed to make the DCBA a common standard. However, with GaN technology, the efficiency and power density requirements for DCBAs are within reach and a new door has been opened to power architecture designers. It should not be forgotten that at one time today’s ubiquitous IBA was considered out of reach for similar reasons.

Summary

This introductory chapter began by showing how the performance of low-voltage power converters dominates system efficiency, and why low-voltage is the most promising area for reducing energy usage in data center and telecom power systems. This discussion was followed by a review of existing power architectures and their properties, and ends with a brief introduction to a promising new power architecture.

The remainder of this book shows how the dramatic increase in switch performance of GaN compared to silicon not only permits vast improvements in existing IBA converters, but also prompts a fresh look at changing power conversion system architecture. The following chapters present real-world evidence of the benefits of gallium nitride technology in IBAs using the following design examples:
48 V – 12 V isolated IBCs – regulated

48 V – 12 V isolated IBCs – unregulated

48 V – 12 V non-isolated IBCs – regulated

12 V – 1 V non-isolated POL converters

48 V – 1 V non-isolated POL converters

References


Also see:
- DC-DC Converter Handbook: The latest design insights using GaN transistors