Cell-aware test can be “Awarding”

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Friedrich Hapke, Director of Engineering for Tessent Solutions, Mentor Graphics, received the Bob Madge Innovation Award at the 2015 IEEE International Test Conference (ITC) for Cell-Aware Test. This award honors innovators in semiconductor, test, and data analysis for exemplary research that changes the industry and challenges existing approaches. This is the first year for the award that honors the memory of Bob Madge (1963-2014). Mr. Madge was an innovator that shared what he learned and encouraged others to rise above the norm and to innovate.

After the ceremony, a thought crossed my mind: the test community should know the inside story of Cell-Aware Test (CAT). So I sat down with Friedrich to discuss his thoughts about the award and to ask him questions that provide his unique perspective on CAT.

Did you know Bob Madge? What were your feelings when your name was announced as the winner of the award?

Sadly, I missed out on meeting Bob in person. But, I have read many of his papers and I have to say that I am inspired by the way Bob shared results from his research and by his impressive work in the design-for-test field. When my team and I first learned about the award, we strongly felt that our work on CAT matched up well with the award criteria. When I was informed by the Award Selection Committee that I was the winner, I was very happy because this award recognizes the innovative research and implementation work that my team and I have accomplished on CAT.

Could you provide a high-level description of CAT?

The CAT approach enables a transistor-level, defect-based automatic test pattern generation (ATPG) on full CMOS-based designs to significantly reduce the defect rate of manufactured ICs, including FinFET technologies. Creating a CAT view is a one-time task performed for each technology node. The CAT views are created by performing analog simulations on each cell within the standard cell libraries. This CAT view is then used by design teams to generate production test patterns that result in significantly higher pattern quality than traditional production test patterns. Traditional fault models fully test the periphery of standard cells and the interconnections between them, but they do miss many bridges, opens, and transistor defects internal to the cells. Advanced process technologies, notably the use of FinFETs, introduce a variety of new failure modes that are addressed by the CAT fault model. CAT also enables Cell-Aware Diagnosis to isolate cell-internal defects that provides guidance for physical failure analysis.
Did you and your team invent this technology? How did the idea come about?

Yes, this technology was invented by myself and my engineering team. While I was working for a semiconductor company in 2007, a colleague of mine was analyzing a high-volume production test of one million tested parts, comparing failing parts from traditional Stuck-at (SA) patterns and Embedded-Multidetect-Deterministic (EMD) patterns. That experiment revealed that there were a few parts that only failed the EMD patterns. Those parts were analyzed by electrical failure analysis and PFA. The analysis isolated one cell type; a simple multiplexer with two data inputs and one select input. The difference between the SA and EMB patterns applied to the multiplexer cells, showed that just one cell input combination (all inputs zero) was missing in the SA pattern set.

After my team and I moved to Mentor Graphics in 2008, I continued exploring this topic further. It became clear to me that a traditional SA ATPG is not forced to generate the missing input condition at the mux inputs. A new technology would be needed to force ATPG to generate all important input conditions to detect real physical defects inside of standard cells. After further, intense thinking about methods to force our ATPG tool to generate complete input conditions, I came up with the idea of using analog simulations to inject physical defects into SPICE netlists that are extracted from the actual layout of the cells. The results of this simulation are used to create a new cell and layout-related ATPG view. This methodology was the genesis of CAT.

Do you and your team hold patents for CAT?

Yes, my team and I were granted two patents for CAT that Mentor Graphics holds: “Cell-Aware Fault Model Creation And Pattern Generation” granted in 2010 and “Cell-Aware Fault Model Generation For Delay Faults” granted in 2013.

What are the key benefits that CAT provides?

A key benefit provided by CAT is the significantly higher quality CMOS ICs delivered from semiconductor companies to their customers, due to the substantial reduction of
defective-parts-per-million (DPPM). An associated benefit to the semiconductor companies is the ability to perform a Cell-Aware Diagnosis that isolates real physical, cell-internal defects in order to guide physical failure analysis and to achieve fast yield ramp-up for new technologies.

**Could you describe the process that semiconductor companies used to validate CAT?**

In the beginning, each semiconductor company kept their SA, Transition, and optional N-Detect patterns and then generated Cell-Aware “topoff” patterns. By doing this, they could log the unique detections from Cell-Aware specific failures and they could determine the successful reduction in DPPM for their products. Today, we have published the results of such experiments with various companies totaling over 50 million tested parts. These experiments show reductions of up to 1,500 DPPM.

**How many semiconductor companies have embraced this technology?**

A large number of companies use CAT and that number increases each year. In “Cell-Aware Test” published in the September 2014 issue of IEEE Transactions on Computer-Aided Design, I acknowledge experts from 12 leading semiconductor companies who validated CAT and who assisted my team by specifying advanced tool features.

**Does CAT augment traditional test models (SA, Transition, and N-detect) or does it eliminate the need for them?**

CAT is a superset of the traditional SA and Transition tests, so CAT eliminates the need for these tests completely. Only by luck does N-detect create some important cell input conditions. But, it entirely misses other important cell input conditions. The Cell-Aware fault model forces ATPG to generate all the required cell input conditions. This means that the need for N-detect patterns is significantly reduced as well.
What is the next area of research to extend the CAT technology?

There are various research topics underway. One example is to attempt to further improve the quality of CAT and the Cell-Aware Diagnosis accuracy by taking Design for Manufacturing (DFM) aspects into account. Other research topics include improving the Cell-Aware view creation process and increasing Cell-Aware ATPG performance, because CAT is quite new when compared to the traditional ATPG technology.

Do you believe there is an entirely new fault model out there, awaiting to be discovered?

Currently, I don’t think that we need another fault model. The Cell-Aware fault model (targeting all cell internal defects) combined with the layout-aware Bridging fault model for detecting defects on interconnects (outside of cells) is fully sufficient. But, I am looking forward to further collaboration with semiconductor companies to learn more about the system level tests (SLT) that they perform. I believe we can use that knowledge to inject these SLT-only detected defect types during the Cell-Aware analog simulations to further improve the quality of CAT patterns and to further decrease the DPPM rates.

Thank you Friedrich for providing a closer look at CAT, its ongoing success, and for providing a peek into the future of test.

References
• “Tessent Cell-Aware Test” whitepaper
• “Cell-Aware Test” IEEE Transactions on Computer-Aided Design