ADC SNR effects due to parasitics, mismatch, and noise

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1. Introduction

Successive-approximation-register (SAR) analog-to-digital converters (ADCs) are commonly used in applications which require medium to high resolution. The major benefits of SAR ADCs are high performance, low power consumption, and small die area.

To reduce the die area, a split-capacitor DAC array is used. The architecture is shown in Figure 1. The split capacitor array works both as a DAC and a sample-and-hold circuit. An attenuator capacitor $C_a$ is used to split the array into two subarrays. After the sampling phase, the output voltage at the array output is $V_{in} - V_{ref}$, where $V_{in}$ is the ADC input voltage and $V_{ref}$ is the reference voltage. During the approximation phase, the output voltage reaches a value of $V_{ref} + V_{qe}$, where $V_{qe}$ is the quantization error. The DAC input leading to this value is the conversion result. But there are sources of error which must be minimized.

![Figure 1: Split Capacitor SAR ADC](image)

2. Sources of error

2.1 Parasitic Capacitance
On every capacitor of DAC array, there is some parasitic cap on both upper plate and lower plate. The parasitic cap on lower plate is not important for SNR calculation because it does not take part in charge sharing during successive approximation process. Value of parasitic cap depends various factors like layout, manufacturing process etc.; plus it varies from die to die.

![Parasitic cap](image)

**Figure 2: Parasitic cap**

### 2.2 Mismatch between capacitors

It is impossible to create capacitors of exact value on die. Like Parasitics, mismatch is also dependent on layout and manufacturing process. Figure 3 shows two capacitors, the second capacitor should have double value of first but its value varies with delta. With proper layout, value of delta as low as 0.1% can be achieved.

![Mismatch](image)

**Figure 3: Mismatch**

### 2.3 Coupling from nearby nets

If adjoining nets to the input or reference voltage are switching then they may couple noise. Figure 4 shows the input sine wave; noise coupled to the sine wave from nearby net can be seen in magnified snapshot.
3. Analysis

To study the impact of various factors on SNR of ADC, behavioral model [2] was used. In every simulation 1024 samples of sine wave were taken and converted to 12 bit digital value and then SNR was calculated. 1000 of these simulations were performed and finally RMS value of all SNR values was taken.

The output voltage of the DAC can be calculated as follows:

\[
V_{\text{out}} - V_{\text{ref}} = \left( \frac{C_{\text{sumL}} + C_{\text{pl}} + C_a}{\left( \sum_{i=0}^{N-1} 2^i \beta_{11}^i C_0 \right)} \right) \cdot \left( \frac{\left[ C_{\text{sumL}} + C_{\text{pl}} + C_a \right]\left( C_{\text{sumM}} + C_{\text{pm}} \right) + C_a \left( C_{\text{sumL}} + C_{\text{pl}} \right)}{\left( \sum_{i=0}^{N-1} 2^i \beta_{11}^i C_0 + C_0 + C_{\text{pl}} \right)} \right)^{-1}
\]

Where \( C_{\text{sumL}} \) is the total capacitance of the LSB half of the array and \( C_{\text{sumM}} \) is the total capacitance of the MSB half of the array. \( N \) is the number of bits used by the DAC, \( C_0 \) is the unity capacitor value, and \( \beta_{11}^i \) is equal to the corresponding DAC bit of the MSB half of the array.

SAR algorithm is run for conversion and above equation is used to find \( V_{\text{out}} \) by switching bits one by one from MSB to LSB.

3.1 Impact of parasitic cap on SNR

Random value (between 0 - Max (%)) of parasitic cap for each capacitor was generated in every simulation. 1000 such simulation were performed and finally RMS value of SNR was calculated. Figure 5 shows the variation of SNR with parasitics, the value of parasitic in the table is the max possible value of parasitic cap. We can see that just 0.2% parasitic cap can result in a 6dB SNR drop.
3.2 Impact of Mismatch

Here also for different max values of mismatch, random values are generated for each capacitor and then conversion is done. 1000 such conversions are done and finally RMS value of SNR was calculated. A 0.1% mismatch between capacitors degrades the SNR by 3.2 dB.

3.3 Impact of coupling

Here we take random values of noise (from 0 - Max) which is added to input signal value. For every conversion there are 1024 samples so 1024 different values of noise are added in every conversion and 1000 such conversions are done and then RMS value of SNR was calculated.
4. Conclusion

The above analysis shows how a small mismatch in capacitance, parasitic capacitance, or noise coupled from nearby nets, can degrade the performance of a SAR ADC. This high sensitivity makes it imperative to properly match capacitors at the layout stage and use various calibration techniques in the on-chip SAR algorithm to improve its performance. Shielding ADC nets can help to avoid the noise coupled which will again help to improve performance.

References
