PAM4: A new measurement science

Martin Rowe - December 01, 2015

This article is part of EDN and EE Times’ Hot Technologies: Looking ahead to 2016 feature, where our editors examine some of the hot trends and technologies in 2015 that promise to shape technology news in 2016 and beyond.

As the world's insatiable appetite for data keeps growing, engineers must continuously develop new technologies to move bits ever faster. With 100 Gbps serial links in rapid deployment, engineers are under pressure to develop the next higher speed: 400 Gbps Ethernet and others are beginning to take shape. But, the shape of the waveforms looks to be quite different this time.

With previous speed increases, engineers have found ways to keep using the traditional NRZ (non-return-to zero) modulation where one baud carries one bit. But as individual links move from 25-28 Gbps to 50-56 Gbps, NRZ could be reaching its limit. That's because the bandwidth required to carry NRZ could just be too much to be cost effective. Plain old PCBs just can't handle it, making signal losses intolerable. NRZ just might be running out of steam. Of course, we've heard that before.

Enter PAM4 (four-level pulse-amplitude modulation) a topic of two panels and nine technical papers at DesignCon 2016. PAM4 should let you develop 56 Gbps data lanes with less signal loss than would occur by simply doubling the NRZ—sometimes called NRZ-PAM2—bit rate. Exotic PCB materials can compensate for the deficiencies, but at a cost few are willing to pay. PAM4 doubles the bit rate for a given baud rate over NRZ. Thus, a 28 Gbaud PAM4 signal can deliver the same bit rate as a 56 Gbaud NRZ signal. Figure 1 shows the difference between NRZ (left) and PAM4 (right).

Figure 1 An NRZ data stream (top left) uses two voltage levels and produces a single eye (bottom...
Besides the bandwidth advantage, PAM4 can result in the need for fewer PCB traces. At 56 Gbps, 400 Gbps Ethernet can be realized with four lanes of PAM4 but might require eight 28 Gbps lanes with NRZ. Thus, PAM4 can reduce the traces in half, reducing the risk of crosstalk and making a PCB designer’s job easier.

There’s more than one way to encode bits onto a PAM4 signal. Figure 2 shows one possible coding of bits; this one uses a Gray code. The goal of an encoding scheme is to minimize the number of bit transitions, which can improve signal integrity.

![Grey Code And/Or Mapping](image)

**Grey Code: 3201**
- 01
- 00
- 10
- 11

**Figure 2** This simulated PAM4 eye shows how the signal might be coded to get four levels and thus two bits per baud. (Image courtesy of SiSoft)

Lower bandwidth means less loss at a given frequency and fewer PCB circuit traces. That’s the good news. The bad news is that PAM4 trades off bandwidth for SNR (signal-to-noise ratio). That makes PAM4 eyes more sensitive to noise than NRZ eyes. "Because it has three eyes, PAM4 divides SNR by three as compared to NRZ," noted Patrick Connally, Technical Marketing Engineer, High Bandwidth Oscilloscopes at Teledyne LeCroy. As a result, PAM4 receivers will need three slicers to detect the eyes, as Figure 3, from a DesignCon 2015 paper, shows. The additional slicers add complexity and cost to receivers.
A PAM4 receiver will need three slicers to detect the three eyes.

There are other tradeoffs, too. Take a look at the simulated PAM4 signal in Figure 2. In the middle eye, the widest point is at half the eye’s amplitude. But, that’s not the same for the upper and lower eyes where the widest eye opening may occur at about the 1/3 or 2/3 point in the eye amplitude. The compression occurs because rise and fall times have finite speeds, cutting off parts of the eyes. The nonlinear eyes can result in DDJ (data-dependent jitter), a form of intersymbol interference.

Another issue with PAM is timing skew. In figures 2 and 3, the simulated eyes are perfectly aligned in time, stacked directly on top of each other. Figure 4 shows that’s not always the case with real signals. Skew can occur, making the eyes even more difficult to properly detect.

Real PAM4 signals may be subject to skew. In this case the, upper and lower eyes lag the middle eye. (Image courtesy of Teledyne LeCroy)

While timing skew can occur in purely electrical signals if trace lengths are not the same, it's more prominent when the signals pass through optical links. Steve Sekel, Strategic Product Planner at Keysight Technologies, explained that "timing skew occurs when you excite a VCSEL (vertical-cavity-surface-emitting laser) and directly drive the laser. Assume, for example that we designate the four signal levels as 0, 1, 2, 3 from bottom to top. A level 2-3 transition will arrive at the receiver faster than 0-1 transition because it starts at a higher voltage."

These and other issues are forging new techniques for how to measure PAM4 signals. "One to two years ago, customers started coming to us asking what could we measure regarding PAM4," said Connally. "We asked them what did they want to measure? The first thing we had to do was to see if we could trigger our oscilloscopes on a PAM4 signal. Creating an eye diagram requires that the
oscilloscope recover the clock from the data. We found that we could get reliable triggers by using our NRZ clock-recovery and trigger algorithms."

**Detecting bits and bit errors**

While it's true that oscilloscopes (and receivers) need to recover embedded clocks from incoming signals, it's just a first step in detecting bits and bit errors. Remember, all these signaling issues come down to bit errors. One such tool used to calculate bit errors is the bathtub curve. Because of the three eyes in a PAM4 signal, simply generating the traditional bathtub curve used for NRZ isn't enough. **Figure 5** shows that you'll need both horizontal (timing) and vertical (voltage) bathtub curves.

The timing bathtub curve on the right is nothing new. It's been used to show a horizontal eye opening at a given BER (bit-error rate). The curve on the left shows that with PAM4, you'll have to look at vertical eye openings at a given BER. Furthermore, you'll need pair of bathtub curves for each eye.

**Figure 5** PAM4 signals will need both horizontal and vertical bathtub curves that look at both eye height and eye width as a function of BER. Source: OIF's CEI 56G Interfaces – Key Building Blocks for Optics in the 400G Data Center.

(Image courtesy of Optical Internetworking forum)

The smaller eyes in a PAM4 signal will also force transceivers to use more error correction than they need with NRZ. Without sufficient equalization, BER will be far too high to make PAM4 signals useful. The simulation in **Figure 6** shows how using **DFE (Decision feedback equalization)** and **CTLE (continuous time linear equalization)** in receivers can improve eye openings. **FFE (feed-forward equalization)**, used in transmitters, can further improve eye openings.
Although the PAM4 concept isn’t new, it’s been used mostly in academia and research labs. But with 400 Gbps Ethernet in development, PAM4 is moving out of the lab and into industry. “Adoption of PAM4 will depend on how long 100 Gbps Ethernet stays hot,” said Chris Loberg, Senior Technical Marketing Manager at Tektronix. "PAM4 is still in the innovators stage," he said. "Before PAM4 can reach 'The Chasm,' it will need standards for both design and test." See Figure 7.

Long-reach Ethernet appears to be moving towards PAM4. Indeed, the OIF is on the verge of specifying it for several 56 Gbps standards that will combine to form 400G Ethernet. Table 1 shows that some standards will be developed for both NRZ and PAM4, leaving the door open in case NRZ proves feasible for 56 Gbps lanes. For 56G-LR, NRZ is out of the running.
PAM4 will be a hot topic at DesignCon 2016. You can practically spend the entire conference learning about it. "Even with all the attention PAM4 is getting," noted Doug Burns, Vice President/Director Support & Consulting Services at SiSoft, "It's still not a slam dunk."

The links below take you to DesignCon session descriptions:

- The Case of the Closing Eye - Resolving 25Gb/sec Design Challenges
- A Tutorial on PAM4 Signaling for 56G Serial Link Applications
- PAM4 for 400 Gbps: acquisition, measurement, and signal analysis
- Channel operating margin for 56 Gb/s PAM4 chip-to-chip and backplane interfaces
- 100GBPS Dual-Channel PAM4 Transmission Over Datacenter Interconnects
- PAM-4 Simulation to Measurement Validation with Commercially Available Software and Hardware
- IBIS-AMI Based Link Analyses of Realistic 56G PAM4 Channels
- Jitter, Noise Analysis and BER Synthesis on PAM4 Signals on 400 Gbps Communication Links
- ISI Tolerant Signaling: A Comparative Study of PAM4 and ENRZ
- Updates on measurement solutions for PAM-4 signaling
- The challenges of measuring PAM4 signals

Also see:

- The next generation's modulation: PAM-4, NRZ, or ENRZ?
- Is PAM4 ready for prime time?
- Oscilloscope makers demonstrate PAM4 eye diagrams
- When will PAM4 take over from NRZ?
- PAM4 takes the spotlight at DesignCon 2015
- Friday Quiz: PAM4 Modulation

Also watching:

5G: With everything going wireless, 5G will be needed to keep up with demand. Several test companies have announced equipment for characterizing air interfaces, any of which could turn into those that ultimately get adopted by standards bodies and wireless carriers.

Instrument user interfaces and the invasion of touch screens and pinch gestures: Although our test and measurement market survey shows that engineers still prefer knobs and buttons you can't help but notice the oncoming wave of instruments that use virtual front panels.

USB 3.1 Gen2: Data rates of 10 Gbps, power delivery to 100 W, and completely reversible Type-C connectors have set up USB 3.1 Gen2 to do what USB 2.0 did to USB 1.1. As with any sweeping change, testing USB gets much more complicated.
Merging of test equipment: Oscilloscopes get function generators, DMMs, and spectrum analyzers in addition to being logic analyzers. It's a bench-saving change in test.

Power and energy: With the every-stronger need to cut power consumption, improve battery live, and cut greenhouse emissions, test equipment is responding to the need for better accuracy and higher resolution. Several new power analyzers appeared on the market in 2015. Expect that trend to continue.

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- Embedded security taking root
- Energy harvesting for high power
- Environmental compliance 2016: Safe world, strong business
- Galvanic skin response stimulates wearable electronics
- High stakes in broadband satellites race
- IoT networks heat up
- LED lighting: More intelligent, more beautiful, more affordable
- Sensor-rich ADAS speeds up
- Software-defined power brings to bear critical need in modern power systems
- The year of 3D memory
- Voice-activated interface becomes pervasive and persistent
- 2D semiconductors take aim at optical communications
- 2016: The year of the nanotube transistor?

Want more PAM4? Attend DesignCon 2016, the premier conference for chip, board, and systems design engineers. Taking place January 19-21, 2016, at the Santa Clara Convention Center, DesignCon will feature technical paper sessions, tutorials, industry panels, product demos, and exhibits. Register here. DesignCon and EDN are owned by UBM.