The latest advances in automotive and Internet of Things (IoT) devices continue to drive the complexity of today’s mixed-signal designs, significantly challenging mixed-signal verification. Engineers require solutions that span from transistors to chips to systems, and they also need better ways to improve productivity. This article will examine the key trends, challenges, and emerging solutions in mixed-signal system design enablement, focusing on mixed-signal verification.

Taking a system-level view of automotive design

Approximately 85% of SoC design starts are mixed-signal designs, according to IBS, and many of them also require low power consumption. Automotive designs provide a good illustration of an industry where engineers are facing more system-level design challenges. In years past, a typical automotive design would have simple microcontrollers and a single sensor. Now, particularly with the rise of autonomous driving, infotainment systems, and advanced driver assistance systems (ADAS), vehicles have multiple sensors and MCUs that may need to talk to each other.

At the device level, these chips must be simulated, and verified that they can operate reliably under extreme environmental conditions. At the system level, the vehicle must be designed so that it will respond to all of the sensor inputs safely. For example, engineers must ensure that sensor data can be aggregated and analyzed to present an accurate picture of what is happening, whether the vehicle needs to detect a jaywalking pedestrian or an errant lane change by another car. IP, design tools, and other components in the supply chain must be certified to meet vehicle functional safety standards, such as ISO 26262.

Power hasn’t been a big concern in automotive design, as the vehicle battery has generally been sufficient to provide the power needed by in-vehicle electronics. However, cars now commonly contain hundreds of sensors, feature in-vehicle connectivity via wireless protocols, and also boast redundant sensors and systems for reliability. More low-power design techniques need to be incorporated to reduce the total power consumption of the electronic system. The power distribution system, particularly for electric cars, might at some point require a redesign in order to provide enough power to accommodate all of these sources.

One surprising trend that is underway for the automotive industry is a shift to advanced-node SoCs. Larger process nodes have long been sufficient for automotive SoC designs. However, since automotive sensors are aggregating so much more data these days, powerful processors are needed to analyze this data and make real-time determinations. What’s more, the volume of data is likely to grow—future cars will probably need to be able to communicate with other cars, for example. Advanced-node chips would provide the processing speeds to support this.
Lowering power of IoT designs

IoT designs encompass a broad array of end devices, all requiring connectivity. Power consumption is an extremely critical element in field sensors and wearable devices. To meet the stringent low-power requirements, many engineers are turning to techniques such as ultra-low power design, via sub-threshold CMOS design, and the integration of elaborate power-management control systems. These techniques require better characterization of devices at low voltage levels, with special attention paid to process variations and leakage power. Foundries are developing processes specifically targeting ultra-low power designs.

Energy harvesting also presents a promising future option. The photovoltaic method is currently the most common method. Energy harvesting from radio or sound waves remains in the research phase. Currently, the amount of power being harvested from those new methods is fairly low and may not be sufficient for ultra-low power designs.

Like automotive, IoT designs, too, are driven by large volumes of data that need to be aggregated and analyzed. In IoT gateways and cloud servers, performance and connectivity features are critical to success. Advanced-node processes are a playing an important role in providing sufficient computing power. Foundries are continually driving towards sub-10nm process nodes. However, advanced-node processes can only push things so far. Many engineering teams are also tapping into 2.5D and 3D technologies to combine chips with different technologies through advanced packaging. This not only extends Moore’s Law, but also can take advantage of multiple process nodes to optimize device performance.

All of these methods and technologies lead to more complex verification of chip, package, and board—and a need for better analysis tools to ensure signal integrity and power integrity, model thermal effects, and more. It’s also more important to look at a design holistically (Figure 1), to be able to simulate the chip with the package and the board as an entire system.

![Figure 1: A holistic approach to chip design—taking into account chip, package, and board—can support a more comprehensive verification process.](image)

Improving mixed-signal verification productivity

Typically, mixed-signal methodologies have entailed a long journey. For example, consider a sensor company whose designs may initially have very few digital components. As these designs grow more complex, the design team must handle an increase in digital content. Treating the digital content the same as the analog is not only costly, but also doesn’t yield the best results. As a result, the
engineers must learn new methodologies and adapt their skill sets.

On the tools side, this shift involves merging analog and digital methodologies to support design of high-quality chips. While there isn’t a one-size-fits-all flow that works with all mixed-signal designs, there are some essential points to consider. First off, front-end verification starts with simulation, when you can co-simulate both the analog and digital sides together. Speed is an important goal here, but also presents a challenge. On the analog side, a SPICE solver is traditionally used, but it is slow for the digital side. On the digital side, verification generally consists of functional verification of the whole chip. However, with mixed-signal designs, engineers are often forced to plug a SPICE engine into the functional verification process, slowing everything down. You need to have regressions and to be able to run thousands of simulations every night, but the SPICE solver doesn’t support the speed required to get through such a volume of simulations.

How can we efficiently model analog in a digital world? Many are turning to SystemVerilog real number modeling, creating a model of the analog block to accurately and quickly represent its behavior for full-chip verification. While this option delivers speed, it also means that someone familiar with the design should write the model and then validate its accuracy. Model creation and validation can, thus, become a burden for an analog-centric engineer.

Then the question turns to: how do I know when I’m done? Improving overall design quality calls for a well-documented verification plan, which can help you determine when your design is fully verified. Using a metric-driven verification methodology (Figure 2), along with one of the tools on the market that automates the verification management process, you can track your verification progress on the digital side. Have I done all of the necessary tests? What percent of simulations passed and failed? However, there does not yet exist a similar methodology for the analog side.
Figure 2: A metric-driven verification methodology, when extended to cover analog designs, can benefit mixed-signal design verification.

Methodology shift needed

It’s clear that successful mixed-signal chip verification calls for a methodology shift. Metric-driven verification has to extend to mixed-signal designs. Real number modeling becomes a critical enabler. We’ll see assertions being adopted more frequently in the analog domain as well. Finally, verification planning is a must. All of this necessitates skills and organizational alignments, with organizations hiring dedicated mixed-signal verification engineers as well as engineers with analog behavior modeling expertise.

Summary

As mixed-signal designs continue to grow more complex, a methodology shift is clearly needed to efficiently verify the analog and digital components of an SoC. What’s more, a holistic, system-level view—encompassing chip, package, and board—is needed to ensure high-quality chips for application areas including automotive and IoT.
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