A MOSFET’s behavior on a phase-shifted ZVS full bridge DC/DC converter

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In the last few years, the market request for systems with a high enough efficiency level to manage high power has pushed SMPS designers toward topologies with low electric losses. The full-bridge converter with PWM phase-shift control is one of very popular topologies potentially capable of achieving that efficiency at high power levels combining the advantages of hard switching technology and soft-switching technology. The aim of this article is to investigate the potential electrical stress on MOSFET devices when they are used as switches on a zero voltage switching (ZVS) converter.

Introduction

The ZVS phase shift converter is addressed to the market of power applications like telecom power supplies, main frame computer-servers and any applications where power density and high efficiency are a must. To reach this target, we must minimize power losses and reactive size, and this is possible by increasing the switching frequency of the converter. High switching frequency means more switching losses, which is in opposition to the target of efficiency. The solution is represented by topologies driven to operate ZVS or zero current switching (ZCS) converters. The technique guarantees in the switches that voltage or current is zero before the transition, and in particular, the ZVS guarantees zero voltage across the switching device before turn on, thereby eliminating any power losses due to the simultaneous overlap on the switch current and voltage.

Benefits such as constant-frequency operation with linear control, integration of the stray components in the power circuit, low EMI are opposed by drawbacks like complex phase-shift controller, ringing and overshoot across the rectifier, and loss of soft switching at light load. Recently, the problem of the complex controller has been alleviated by the introduction of integrated controllers while the solution for the light load conditions is offered by a dedicated selection of switches. Some electrical characteristics of the MOSFETs used in the converter can help the system, reducing the failure risk. This article reports the operation sequences where the risk occurrence is most probable.

ZVS Topology description

The basic circuit of the phase-shifted converter is composed of four switches: two for each “leg.” Due to the operation mode, the switching transitions on one leg always happen before the other one. The first is usually named “leading leg” the other one “lagging leg.” In Figure 1, the leading leg is represented by the switches Q1 and Q2 and the lagging leg by Q3 and Q4.
The control of the power delivered is obtained by setting the shift time between the two phases, and in particular, a short time is set to deliver high power while a long one for the low power level. This technique allows control of the powering phase.

Looking the signals sequence reported in Figure 2, it is very easy to understand that the devices in the Q3 and Q4 positions change their states after the complete transition of the other two devices. In other words, devices Q3 and Q4 in the “leading leg” complete their transition from ON to OFF or vice versa always in advance compared to devices Q1 and Q2. Due to the switching sequence, the devices in the “leading leg” are submitted to a freewheeling phase not visible in the “lagging leg.” The sequence is summarized in the following table.
This control technique allows the reduction of the switching losses because the operations are managed so as transitions occur from OFF state to ON only when the voltage across to the devices is zero. In Figure 3, typical waveforms on a Phase-Shift (P-S) ZVS converter are shown.

As highlighted in Figure 3, if attention is focused on Q4 signals and in particular on its current, it is possible to note that it is made up of two parts. In the first part, the current flows through the device from source to drain shared by the channel and body diode, while in the second one, the current flows only inside the MOSFET channel from drain to source. Current inversion happens as soon as voltage across the transformer changes its polarity. Taking advantage of this sequence, the lagging device Q2 is switched during this phase, and then it starts to conduct with its voltage equal to zero realizing the ZVS transition.

Particular attention must be given to the current in the Q4 device. When its current inverts the direction, the voltage applied is low. Since the current is composed of two parts, the time duration (trr) of the removal of the minority carrier in the body diode is lower compared to a typical test. The concentration of the minority carriers is mainly linked to the lifetime of the recombination. For this reason, devices with fast recovery time are usually proposed for this topology. The next section reports the possible failure risks that arise due to this aspect.
Failure risk for switch device

As reported in the previous section, during the ZVS transition, the internal body diode of the MOSFET Q4 is involved in the operation, and its conduction time is fixed by the load level. In order to regulate the power delivered, the shift time between the two legs is variable, and consequently, the body time conduction changes from a short time for high power level to a short time for low load level.

![Figure 4 Typical waveforms with high load](image)

![Figure 5 Typical waveforms with low load](image)

If we compare the two cases, it is clear that in the case with low load level shown in Figure 5, the time available for the recombination is lower compared to the case reported in Figure 4, and it could be less than that requested to complete the operation. Focusing attention to this instant, we see that the light load condition represents the most critical working operation for this kind of risk.

As reported in Figure 6, the red dash lines show different recovery times, and consequently, the case of the potential risk if an improper device is used. Three different lines are reported to simulate three different recovery times. Two of them represent safe cases while the third is a potential case of failure. In the last case, the time available is not enough to completely recover the minority carriers inside the MOSFET.
To reduce the failure risk caused by this electrical stress, MOSFET devices with low \( \text{trr} \) and \( \text{Qrr} \) parameters are selected. Several silicon technologies are presented to solve the above-mentioned failure modes in the ZVS topology, and there are several MOSFET devices with fast reverse recovery time and better \( \text{dv/dt} \) ruggedness suitable for higher frequency ZVS full-bridge applications. This choice is also usually made by the SMPS makers to increase the reliability of their systems.

**Figure 6** Typical waveforms on leading device

**Figure 6** refers to the current waveform on the device placed in the “leading leg.” The same analysis can be done for the “lagging leg” devices. As for the devices in the “leading leg,” the conduction phase of the “lagging leg” devices includes a recovery operation of their internal body diodes. In this case, if the devices selected are the same as those of the “leading leg,” no issue can be observed (**Figure 7**) since there is more time available to the recovery phase than in the previous case.
Conclusions

The document has presented a study of the potential risk for MOSFET devices when used in a P-S ZVS converter. Analyzing the transition sequence of this specific topology, the study has highlighted the critical working operations where failures could happen and the positions in the topology are more sensitive to the electrical stress. Dividing the topology in two sections labeled “leading leg” and “lagging leg” due to the sequence of the operations, some electrical characteristics of the MOSFET are been investigated, and a thesis for the device selection was formulated. The devices have to take into account the constraints requested of the “leading leg” in terms of $t_{rr}$ and $Q_{rr}$. The proper choice allows the improvement of the system’s reliability, reducing the failure risk and obtaining a solid design.

References

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