Proper oscilloscope setup yields correct ESD measurements

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Automotive electronic components are designed to have, and are tested to determine, a certain level of immunity to ESD (electrostatic discharge). The tests address a variety of conditions the components will encounter including packaging, handling, vehicle assembly/service, and intended operation. To properly test any system, subsystem, or IC, you need to measure the voltage waveform used to test a DUT. Unfortunately, typical oscilloscope setups can yield incorrect results. You need to know how to properly trigger an oscilloscope. Plus, you need to get the most from an oscilloscope's vertical resolution to maximize test results.

Automotive EMC (electromagnetic compatibility) specifications typically reference ISO 10605:2008 in describing test setups, procedures, and equipment. Equipment includes an ESD simulator whose components such as the RC networks produce waveforms that represent human ESD models. ISO 10605 also provides a method for verifying ESD simulators. The method assures test repeatability over time and among multiple laboratories and/or ESD simulators from various manufacturers. Proper oscilloscope setup is essential to correctly assess ESD simulator outputs.

ISO 10605 specifies ESD test levels from 2 kV to 25 kV in both polarities. Typically, you apply test voltages in steps by increasing the voltage to an established limit. In addition, you must subject component surfaces, interfaces, and electrical terminals to direct air and contact discharges while unpowered, and while configured and operating in a predetermined mode. The component, while powered, may also be exposed to indirect discharges that produce a radiated disturbance. The component needs monitoring for deviations in operation as well as inspected for damage or degradation of performance upon test completion. Similar procedures are also performed to the full vehicle.

The verification of the ESD simulator includes characterizing the discharge pulse waveform. The second edition of ISO 10605 identifies rise time, first peak current, current at t1 and current at t2 as the parameters of interest (Figure 1). The values of t1 and t2 vary with the value of R and C in a given RC network for the purpose of verifying its time constant.
Figure 1. Measurement parameters of interest include rise time, first peak current, current at $t_1$, and current at $t_2$ on the ESD pulse.

Figure 2 shows an ESD simulator gun applying a contact discharge into a current shunt target that is connected to the oscilloscope’s 50 O DC coupled input through a double shielded cable and inline attenuators. (A detailed description of ESD simulator operation can be found here).

Figure 2: An ESD gun discharges into a current shunt target. The resulting pulse waveform is captured and measured with an oscilloscope.

Although this measurement is a standard requirement, it’s often inaccurately performed because of the oscilloscope's threshold setting and vertical sensitivity. Traditional pulse measurements require an oscilloscope to find the steady-state high and low values of the pulse and then compute pulse parameters such as rise time based on these steady state levels. A problem occurs when using industry default measurement thresholds.
The red histogram in Figure 3 identifies the Top and Base of a waveform. For clock signals, the default thresholds automatically identify the 0% and 100% levels of a waveform, and timing measurements such as rise time are correctly calculated for a clock waveform.

This method for threshold placement is, however, incorrect when applied to an ESD pulse. In this case, the standard IEEE Top and Base thresholds will misidentify the 100% threshold at the semi-stable portion of decay labeled as “top” in Figure 4 and will also misidentify the 0% threshold as the prolonged decay area labeled “base” rather than using the Zero Volt and Maximum ESD pulse values required in standards IEC 61000-4-2 and ISO 10605. Because these standards require that the 100% threshold to be placed at the Maximum level of the waveform, and the 0% threshold to be placed at the Zero Volts level, default threshold placement will result in an erroneous rise time calculation of an ESD pulse.
Oscilloscopes will, by default, misinterpret the prolonged decay area of the pulse, highlighted with a dashed red line in **Figure 5**, as being the 100% steady-state Top level of the waveform (and the peak of the waveform misidentified as being overshoot). Using default thresholds, the oscilloscope will incorrectly calculate the pulse's rise time. Considering the vertical distance between the dashed red line and the solid green line of Figure 5, is it easy to envision how the rise time could be miscalculated with an error margin between 100% and 800% error, relative to EMC standard specification requirements. A critical step to prevent this measurement error from happening is to configure the automatic thresholds to instead be the Zero Volt level and the waveform Maximum level, as shown circled in green.

![Figure 5: Desired ESD pulse threshold](image)

**Figure 5. The desired ESD pulse threshold is identified with a green line, and the default threshold is illustrated with a dashed red line on this acquired ESD pulse.**

**Maximize dynamic range**

The second most common source of inaccuracy in ESD pulse measurements is the selection of volts per division. **Figure 6** shows how an oscilloscope first amplifies the analog input signal (in this case an ESD pulse) in the analog amplifier stage and then outputs the signal to the ADC (analog-to-digital converter). The oscilloscope's dynamic range is determined by the range of signal amplitudes that the ADC can process effectively. The minimum of the range occurs where signal power equals noise power. The maximum of the range occurs at or near full scale where maximum counts of the ADC are used while digitizing the waveform and distortion is minimized.
Figure 6. The ESD pulse needs to occupy most of the vertical range of the oscilloscope's amplifier stage to maximize dynamic range.

If an ESD pulse is acquired while occupying only half of the vertical scale of the screen, then the acquired waveform will lose one bit of resolution (and half of its dynamic range) impacting both vertical and horizontal measurements on the waveform. Horizontal measurements are directly impacted by timing uncertainty at measurement points from spurious noise.

Many oscilloscope users aren't aware that for all available digitizing oscilloscopes, the vertical resolution of an acquired waveform on the display screen is proportional to the percentage of the screen vertically occupied by the waveform.

Figure 7 shows an ESD pulse acquired full-scale, vertically occupying the full grid. This acquisition minimizes quantization noise. Because quantization noise of an acquired waveform impacts both vertical and horizontal measurement accuracy (therefore affecting measurements such as rise time), the scaling of an acquired ESD pulse is essential.

Figure 7. The ESD pulse needs to occupy most of the vertical range of an oscilloscope's amplifier stage to maximize dynamic range.

Figure 8 shows the same ESD pulse acquired while occupying only half of the grid's vertical space.
A typical benchtop oscilloscope in an EMC lab contains 8-bit ADC hardware, which has \(2^8 = 256\) quantization levels. When only half of the vertical range of the display grid is utilized, this results in only half of the ADC range used when the signal is supplied from the analog amplifier output stage (recall Figure 5), and the other half of the ADC range acquiring nothing. Therefore, only 128 quantization levels of the ADC are used, resulting in \(128 = 2^7\) = 7-bit resolution on the acquired ESD pulse.

![Figure 8](image8.png)

Figure 8. An ESD pulse occupying half of the vertical range of the grid loses one effective bit during acquisition, resulting in loss of vertical and horizontal measurement accuracy.

Figure 9 shows the same ESD pulse acquired while the pulse occupies only one quarter of the display grid, resulting in only \(\frac{1}{4}\) of the dynamic range of the oscilloscope being applied to the signal. When using one-fourth of the dynamic range, which uses just 64 of the 256 quantization levels to acquire the ESD pulse, or \(64 = 2^6\) = 6-bit resolution on the acquired ESD pulse. The loss of vertical resolution results in increased quantization noise impacting both vertical and timing measurements, which can have a critical effect on ESD pulse rise time measurements. That's based simple on the operator's selection of \(V/\text{div}\) setting used during acquisition.

![Figure 9](image9.png)

Figure 9. An ESD pulse occupying one quarter of the vertical range of the grid loses three quarters of the ADC range and loss of two effective bits during acquisition, resulting in significant quantization and measurement error.
For this reason, vertical scaling of any digitizing oscilloscope should be set to maximize the ESD pulse shape vertically within the display grid as shown in Figure 7. This often overlooked step has a profound impact on signal integrity and ESD pulse measurement results.

Note that for RC networks where R=2 kΩ, the ratio of the first peak current to the current at $t_2$ is 25:1. This is the largest ratio of measured amplitudes in a single waveform capture during verification and provides a great case for taking full advantage of an oscilloscope's dynamic range.

In summary, two of the most common pitfalls in ESD pulse measurement can be avoided when the oscilloscope operator becomes aware of them. The default threshold measurements of Top and Base must be changed to 0 V – Max to avoid incorrect automatic threshold placement, and the vertical scaling of the ESD pulse used during verification should fill most of the grid vertically in order to maximize dynamic range and signal integrity.

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Also see

- Understanding and comparing the differences in ESD testing
- Detecting ESD Events
- Check ESD simulators first
- Circuit protection: Understanding differences in the Human Body Model and IEC 61000-4-2 standards
- Revised waveform drives ESD standards