Trimming a digital-to-analog converter to improve accuracy

Rahul Prakash, Product Definer and Kunal Gandhi, Product Marketing Engineer Precision Analog, Texas Instruments - September 01, 2016

More and more of today’s modern industrial systems are requiring high accuracy. Traditionally, the test and measurement market has been the primary driver of highly accurate signal chain components, but now this trend is seeping into other markets such as factory automation, optical networking, and medical. Applications such as automated test equipment (ATEs), data acquisition cards (DAQs), and high-performance oscilloscopes require the highest accuracy signal chain.

Precision digital-to-analog converters (DAC) are an integral part of the signal chain and are the primary facilitator of highly accurate signals. The precision DAC is typically used to fine-tune gain and offset, and minimizes other non-linearity. Therefore, it becomes the precision DAC that makes a signal precise as the DAC calibrates the signal. In this article, we talk about two different DAC architectures: R2R ladder and string DACs. Further, we analyze techniques that can help to enhance accuracy in both architectures.

Accuracy in precision DACs

There are many non-idealities associated with any analog integrated circuit, and precision DACs are no different. The main source of direct-current (DC) errors in a precision DAC are offset error (OE), gain (GE), and integral non-linearity (INL). Offset error describes an offset or shift in the entire transfer function across the linear region of operation (Figure 1). Gain error describes the deviation from the ideal slope of the transfer function defined as a least significant bit (1 LSB), as shown in Figure 2. INL describes the deviation between the ideal output of a DAC and the actual output of a DAC. For example, Figure 3 shows an actual DAC output and an ideal DAC output for a simple 3-bit DAC.
Figure 1 DAC offset error of a simple 3-bit DAC.

Figure 2 DAC gain error of a simple 3-bit DAC.
A measure of a DAC’s accuracy must include all three errors. The term total unadjusted error (TUE) is often used to quantify DAC accuracy. TUE is the root sum square (RSS) of these errors, equation (1), as these errors are uncorrelated.

\[
TUE = \sqrt{OE^2 + GE^2 + INL^2}
\]  

The offset and gain errors are often calibrated on the system using a simple calibration scheme. The INL error, on the other hand, requires an extensive calibration scheme that involves many codes. This is a significant burden on the software and requires more memory bits (to store coefficients). Therefore, minimizing the DAC’s INL is the key to enhancing accuracy.

**INL in DAC architectures**

The most common DAC architectures are R string- or R2R ladder-based topologies. The biggest contributor to INL for these DACs is mismatches in resistors used in ladder and string formats. Many analog processes include a high-precision resistor to design ladders and string. As the demand for higher accuracy keeps increasing, having a high-precision resistor is insufficient. To address this concern, additional design, layout, and trimming techniques are being employed to counter the effect of these mismatches in resistors. This is where choosing either an R2R ladder or R string architecture plays an important role in the DAC’s overall accuracy.

**R string**

A typical R string DAC, evident by the name, uses a string of resistors between the reference and ground to generate a voltage corresponding to a digital input. Switches tap out this voltage to an output buffer, which provides the drive capability to the DAC. For example, **Figures 4 and 5** shows...
a DAC R string architecture.

Figure 4 Example of a DAC architecture
Note that a 16-bit DAC needs $2^{16}$ resistors in the R string. Typically, the R string is divided as a most significant bit (MSB) string and a least significant bit (LSB) string. Nonetheless, all of these resistors are required to be matched with each other in order to get the lowest possible INL. Innovative layout techniques along with appropriate sizing can improve matching among these resistors.

**Figure 6** shows an INL versus code plot for a DAC that is string-based, such as the DAC8554.
In their simplest form, R2R ladder-based DACs can be used to implement N-bit resolution DACs. The simplest implementation of a R2R ladder DAC has N-2R resistor legs with switches between a VREF and REFL or GND, a single 2R termination resistor, and (N-1) R-value bridge resistors between each switched 2R leg. A total of (3N+1) R unit value resistors are required for an N-bit resolution R2R ladder. The output buffer (if included) provides necessary load capability to the DAC. It is clear from the architecture that a binary-weighted R2R ladder structure requires one R2R leg for 1 bit. This is significantly lower than the number of resistors required for a comparable R string DAC. Figure 7 illustrates a simple 4-bit R2R ladder structure.
While you can determine the resolution of the R2R ladder-based DAC by the number of 2R resistor legs in the array, you can determine DAC accuracy by the array resistance matching. Array MSB legs are more sensitive to matching requirements while LSB legs are progressively less sensitive to mismatch. Each resistor leg matching sensitivity decreases by a factor of two, moving from each MSB leg progressively down to the LSB leg.

Trimming for accuracy

**Figure 8** shows a typical 16-bit, DAC-based on R2R ladder. Note that a certain number of upper (MSB) bits are segmented (thermometric weighted). This can be found in most data sheets by looking at ladder structure.

![12-bit R2R ladder structure](image)

Trimming for accuracy refers to adjusting the absolute value of resistors in R string and R2R ladder architectures. As stated earlier, INL is the biggest obstacle in achieving high accuracy, and trimming for it is the most feasible option. Trimming an R string DAC is prohibitive due to the large number of resistors. The R2R ladder overcomes this hurdle since the number of resistors to trim is much less.

To trim the R2R ladder (see **Figure 8**); begin with the first lower LSB bit that requires trimming. Typically, for a 16-bit DAC with data bits S0 (LSB) to S15 (MSB), assume that the first trimmed bit is S5. The trim routine looks at the error between adjacent codes 32 to 33. Ideally, the voltage change difference between adjacent codes will be 1 LSB. Assuming that the trim is bi-directional, adjust the error for S5 either up or down, depending on the initial error.

Upon completing the trim for S5, add the delta amount trimmed to all major carry errors for bits above S5 (for example, S6, S7, and so on). Continue this procedure until you reach the MSB major carry bit code. Slight variations in this procedure could be if there are any thermometric decoded MSBs, in which case you would also trim the thermometric decoded major carries, starting at the lowest and moving to the highest. At the end of this trim, the DAC exhibits 16-bit monotonicity, and also achieves sub 1LSB INL. For example, the DAC INL in **Figure 9** (DAC80004) is now a R2R-based DAC.
Figure 9  A DAC with a linearity error versus a digital input code.

Summary

Precision DACs occupies a prime position in the signal chain as it facilitates accuracy. For applications demanding high accuracy, it is imperative to consider the right DAC architecture for the job. R string-based DACs, such as the DAC8554, offers a valuable option for general purpose applications, but they fall short when high accuracy (1LSB INL) is required. As an alternative, R2R ladder-based DACs, such as the DAC80004, are better suited to accuracy-demanding application. This is because the R2R ladder design allows a practical trimming option to achieve ultra-high accuracy (<1LSB INL).

About the authors

Rahul Prakash is a product definer for Texas Instruments’ Precision Analog Data Converters group. He holds an MS in Electrical Engineering, majoring in microelectronics, from the University of Texas at Dallas. He has authored multiple papers in leading technical journals and conferences on analog circuit design techniques and holds three U.S. patents related to analog circuit design and technology.

Kunal Gandhi is a product marketing engineer for Texas Instruments’ Precision Analog Data Converters group. Prior to becoming a product marketing engineer, Kunal was a mixed-signal design engineer for seven years. He has received his MSEE degree from University of Southern California, and an MBA from University of Texas at Austin.

Additional information

1. Check out these TI Analog Wire blog posts:
   - To learn more about OE, GE and INL parameters: "DAC Essentials: How accurate is your DAC?"
   - To understand the resistor string architecture: "DAC Essentials: String theory."
To understand the R2R ladder architecture: “DAC Essentials: The resistor ladder.”

Download applications of precision DACs from the TI Designs precision reference design library.

2. Take a look at the resources in the Precision DAC Learning Center, which includes information for beginners, intermediate level and advanced designers.

3. Watch the Lessons for Precision DACs training series for more information on precision DAC architectures:
   - What is a String DAC?
   - Understanding the String DAC architecture
   - What is an R2R DAC?
   - Understanding the resistor ladder with precision DACs

4. Download these data sheets: DAC8554 and DAC80004