Spacecraft data handling using ARM-based processors

Rajan Bedi - September 27, 2016

Earlier this year I attended ESA and NASA FPGA conferences, SEFUW and MAPLD respectively, and one topic which we discussed was the need for a small, low-power, high performing MCU to replace larger, more dissipative FPGAs. For localised control and processing, such as sensor TT&C or digital control of a voltage regulator, a dedicated MCU would offer a more efficient CPU/DSP option.

Could the solution lie within our cellular phones (smart and not so smart), our tablets, our cars, our IoT devices, and our wearables? Today, almost 90 billion ARM-based chips are being used globally and many of these contain multiple ARM cores. Currently there are over 450 ARM licensees worldwide!

The ubiquitous ARM architecture offers small, low-power, high-performance cores, many of which are being used in safety-critical applications, such as car braking systems, power steering, self-driving vehicles, aircraft, medical, railway and industrial control sub-systems, conforming to fail-safe standards including ISO 26262, IEC 61508, DO-254, DO-178, IEC 62304, IEC 61511/13, IEC 62061, and ISO 13849.

Given that our lives depend on the reliability of ARM-based fail-safe systems every day, could the space industry also benefit from the performance, power, size, ease of use, and accessibility benefits of the ARM architecture? There is a huge, tried and tested ecosystem available to enable developers to build reliable control and DSP embedded applications, e.g. toolchains certified to TÜV SÜD. For safety-critical applications, exception handling is very short and deterministic, and two cores can be lock-stepped to provide redundancy. Further risk mitigation can be implemented at the SoC and system level.

There are a number of options available to allow the space industry to exploit the advantages of ARM’s, small, low-power, high-performance architecture:

1. Several space-grade foundries have licensed the ARM architecture and offer this IP as part of their Hi-REL, ASIC design flow, e.g. ST Microelectronics sells many ARM cores commercially and can harden these for satellite customers baselining its 65 nm, space-grade ASICs.
2. Satellite OEMs can instantiate ARM IP within FPGAs, e.g. users of Microsemi’s ProASIC3 and RTG4 have access to a soft (not placed and routed) 16/32-bit, 60 MHz, ARMv6-M, Cortex-M1 core, which can be implemented using 4,353 logic tiles. Future space-grade FPGAs discussed at SEFUW and MAPLD will allow dual, 32-bit, ARMv7-R, Cortex-R5 cores up to 600 MHz and quad, 64-bit, ARMv8-A, Cortex-A53 cores up to 1.5 GHz.
3. Satellite manufacturers can buy a small, low-power, radiation-hardened chip such as VORAGO’s VA10820 based on ARM's, 32-bit, Cortex-M0 processor.
In this post, I will discuss the third option, the use of a small, low-cost, discrete, space-grade ARM processor to provide localised control and processing functions as shown below.

VORAGO's VA10820 is a radiation-hardened ARM Cortex-M0 MCU.

The **VA10820** is a 60 mW (typical core consumption, 40 mA at 1.5V), -55°C to +125°C, 50 MHz, ARM, Cortex-M0 MCU fabricated using VORAGO's patented, radiation-hardened, HARDSIL technology. The device is packaged in a small, 14×14 mm, 128-pin, ceramic LQFP as shown above.

HARDSIL exploits the benefits of a conductive buried guard ring to eliminate latch-up, reduce circuit noise, and enable high-temperature operation of standard CMOS as illustrated below. The process enhancement does not require any change to the existing fabrication and simply adds several masks to the overall manufacture. The resultant hardened technology inherits all the scaling benefits of the baseline commercial process such as higher performance and lower power consumption in contrast to older, custom radiation-hardened processes.

This is a cross-sectional view of CMOS doping profiles with buried guard rings (BGR), with parasitics depicted schematically.

The buried guard ring increases the holding voltage of parasitic thyristors making it less likely for a latch-up state to exist. If it were to occur, the highly conductive layer underneath the devices prevents trigger by pinning the substrate potential to VSS. HARDSIL substantially reduces the total charge collection initiated by radiation strikes, lowering the occurrence of all types of SEEs. There's
a nice little [video](#) which describes its suitability for harsh environments and there will be a presentation at [ARM TechCon](#) next month.

The Cortex-M0 processor is ARM’s smallest 16 and 32-bit processor containing a three-stage pipeline as well as optimising code density for embedded applications. It has exceptionally low gate count and very low power consumption, e.g. on a 40 nm commercial process, the floor-planned area occupies 0.007 mm$^2$ consuming 5.1 µW/MHz. Its performance is specified as a maximum of 1.27 Dhrystone MIPS per MHz (CoreMark of 2.33).

The [VA10820](#) implements a 50 MHz, ARM Cortex-M0 core with JTAG-based debug connected to 32 kB and 128 kB of on-chip data and program memories respectively via an AHB-LITE bus. A lower-speed peripheral bridge allows access to two UART, two I²C and three SPI interfaces, 54 configurable GPIO as well as control registers.

The VA10820's internal memories contain EDAC protection and all registers include TMR with voting capability. The specified SEL, SEE, and TID immunities are 110 MeV/(mg/cm$^2$), < 1e-15 errors/bit-day (with EDAC enabled) and > 300 krad (Si) respectively. Process reliability and radiation test reports are available from the vendor (or [EBV Elektronik](#) in Europe) as well as an [evaluation kit](#) for representative prototyping as shown below.

HARDSIL technology, based on radiation-hardened Cortex-M0’s and SRAMs, is to be used on the STP-H5 payload to be launched by SpaceX and further parts will enter orbit next year on a GEO mission as well as a LEO spacecraft. VORAGO also offers specific prototyping support for CubeSats.

In terms of future roadmap, VORAGO plans to offer radiation-hardened and high temperature versions of the ARM Cortex-M4 core for space applications. This is based on the full 32-bit ARMv7-M instruction set combining a low-power embedded processor with DSP capability. ARM specifies its
maximum performance around 1.95 Dhrystone MIPS (CoreMark of 3.42).

While there are several other qualified, radiation-hardened MCUs currently available, either single, dual, or quad-core chips or complete, single-board computer sub-systems based on the PowerPC and SPARC architectures, specifications range from 90 to 1800 MIPS (66 to 800 MHz), typically consuming between 1 and 30 W in various packages from 240 to 625 pins.

Today, there is a genuine market need for a tiny, very lower-power and affordable space-grade MCU and a real alternative to small FPGAs for localised control and processing functions. This will also create new opportunities for spacecraft sub-systems, e.g. sensors communicating and networking wirelessly within a reliable mesh. What would you do with lots of autonomous, fault-tolerant, 'chiplet' processing nodes (NASA NNG16574410R)?

I compare the implementation of some space-industry IP on my FPGA training course including VORAGO's VA10820, based on the ARM Cortex-M0 processor, as an alternative to a small programmable logic device. I'd love to hear how you solve your CPU/DSP needs as well as your ideas, and until next month, don't forget to divide your DMIPS by 1757!

P.S. The first person to tell me how this last sentence fits with this post will get a free Courses for Rocket Scientists pen. Congratulations to James from Australia, the first to answer the riddle from my previous article.

Also see:

- Brother, can you lend me an ARM?
- Introducing the world’s first 28nm semiconductor for space
- The definitive guide to ARM Cortex-M0/M0+: Ultralow-power designs
- Are you bored with your board?
- Altera integrates ARM processor in FPGAs
- 10 steps to selecting a microcontroller