Decoupling’s effect on EMC

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It is crucial to understand the impact of decoupling, in term of power distribution network (PDN) impedance on simultaneous switching noise (SSN) and electromagnetic compatibility (EMC). A PCB with poor power integrity or decoupling, e.g., high PDN impedance, gives rise to the issue of SSN and EMC. The next section of this article showcases the practical work that proves the relationship between PDN impedance, SSN, and EMC of PCB.

Analysis and results

Two versions of the following prototype are tested: An FPGA with external 50MHz reference from crystal oscillator, and three major interfaces: DDR2 SDRAM at 350MHz clock rate, ADC data bus at 150MHz, and Ethernet at 100MHz. All these components draw power from a 1.8V buck converter. The test cases listed in Table I are carried out to investigate the effect of decoupling (including PCB stackup and capacitors) on SSN and EMC.

In test case 1, the prototype PCB consists of four signal layers and one ground layer. There are sixteen 0.1µF decoupling capacitors tied to the +1.8V power pins of FPGA on the PCB for this test case. Meanwhile in test case 2, the prototype PCB consists of four signal layers and three ground layers. There are twenty five 0.1µF decoupling capacitors tied to the +1.8V power pins of FPGA on the PCB for this test case.

Table I. Test cases to study effect of PCB decoupling on SSN and EMC
With reference to PDN impedance plot (post-layout power integrity analysis performed using Mentor Graphic Hyperlynx) in Fig. 1, the power net in test case 2 has lower impedance across the wideband range due to its improved decoupling condition compared to test case 1. The 0.1µF capacitors contribute in frequency from low to mid-band (<400MHz). On the other hand, plane capacitance due to ground layers contributes in frequency beyond 400MHz. A lower PDN impedance is experienced by test case 2 due to its higher number of decoupling capacitors and ground layers compared to test case 1.

<table>
<thead>
<tr>
<th>Test cases</th>
<th>PCB stackup</th>
<th>Bypass/decoupling capacitors on FPGA</th>
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</table>
| 1          | layer 1: signal  
layer 2: power  
layer 3: signal  
layer 4: signal  
layer 5: ground  
layer 6: signal  | 1x 100µF;  
1x 47µF;  
1x 4.7µF;  
16x 0.1µF  |
| 2          | layer 1: signal  
layer 2: ground  
layer 3: signal  
layer 4: power  
layer 5: ground  
layer 6: signal  
layer 7: ground  
layer 8: signal  | 1x 100µF;  
1x 47µF;  
1x 4.7µF;  
25x 0.1µF  |

Fig. 1. Plot of PDN impedance

Subsequently, the power spectrum of the +1.8V (probed using spectrum analyzer through AC
coupling) that spans from 30MHz to 1000MHz is compared for both test cases. Referring to case 2 indicated by spectrum in Fig 2b, the spur observed are mainly contributed by the harmonics of crystal oscillator (50MHz fundamental), DDR2 SDRAM (350MHz fundamental), ADC data bus (150MHz fundamental), and the ethernet (100MHz fundamental). The spur with the highest power occurs on the spectrum of test case 1, as shown in Fig 2a, due to poorer decoupling.

The noise on the power net results from the interaction between the PDN impedance and the transient current of the crystal oscillator, and output buffers of ICs that toggle or switch simultaneously at a particular frequency, i.e., SSN. When power impedance is reduced by improving the decoupling, SSN and frequency spurs can be suppressed.

Thirdly, radiated emission (RE) in a 3 meter anechoic chamber is carried out to compare the noise performance between the prototypes of the test cases. Test case 2 shows better RE or EMC compared to test case 1. The larger count of ground planes in test case 2 not only improves the decoupling or PDN impedance, but also provides proper return paths for all the signals that propagate along traces in the PCB. This in turn reduces the RE.

Conclusion

The impact of decoupling on SSN and EMC is demonstrated in this practical work. It is critical that the PDN and stackup of PCB be implemented in a stringent manner to ensure the quality, robustness, and functionality of the prototype.
Reference

[1] "Power Distribution Network Planning", by Barry Olney, In-Circuit Design Pty Ltd Australia


Also see:

- Decoupling’s effect on PI & SSN
- Reducing PDN impedance at high frequencies
- PDN design essentials for wideband low impedance
- Build low-EMI prototypes: The essentials

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