Isolated LVDS buffers for high-speed, high-voltage isolation

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Isolation is a means of preventing direct current (DC) and unwanted alternating current (AC) between two parts of a system, while still allowing a signal and power transfer between those two parts. Isolation is used in a wide variety of applications: to protect human operators and low-voltage circuitry from high voltage, to improve noise immunity, and to handle ground potential differences between communicating subsystems.

Isolators with complementary metal-oxide-semiconductor (CMOS) or transistor-transistor logic (TTL) level inputs and outputs are called digital isolators. You can use digital isolators to isolate two different voltage domains on the same PCB when the signaling to and from the isolator is low speed or limited to a few inches in routing distance.

For high-speed data communication over long board traces or through cables and connectors, low-voltage differential signaling (LVDS) is preferred over CMOS signaling. LVDS offers lower power consumption, lower electromagnetic emissions, better signal integrity (low reflections due to terminated transmission lines) and higher noise immunity over CMOS. When you require isolation in combination with a high-speed interconnect over long distance, isolated-LVDS buffers can provide a compact and cost-effective solution.

Figure 1 shows an example block diagram of a dual-channel isolated-LVDS buffer. Each channel consists of an LVDS receiver and an LVDS driver connected by a digital isolator core.
Isolated LVDS applications

A designer can use isolated LVDS buffers for point-to-point communication between two application-specific integrated circuits (ASICs) or FPGAs. In a high-voltage motor control application, for example, node 1 could be a controller on a safety low-voltage or earth-referenced board; and node 2 could be a controller placed on the power board, biased to high voltage. As shown in Figure 2, you can use the isolated LVDS to provide protective isolation between the high-voltage circuits and parts accessible to human operators.

The LVDS link carries an aggregate of pulse-width modulation (PWM) signals to the isolated insulated-gate bipolar transistor (IGBT) gate-drivers, as well as voltage, current and other feedback from the inverter stage. Hence, high throughput is required from the isolated LVDS link. Also, if the isolated LVDS buffer is the only protection barrier between the high-voltage and low-voltage domains, the LVDS buffer will require reinforced isolation.
A second example (Figure 3) refers to creating an LVDS-based serial peripheral interface (SPI). In this design the interface is between an analog-to-digital converter (ADC) and an ASIC, and the design is used for test and measurement applications. Two Isolated LVDS buffers are used, one in a 21 configuration (one channel in either direction), and the other in a 20 configuration (both channels in the same direction). This solution provides isolation for noise and electromagnetic interference (EMI) robustness, ground loop isolation, as well as protection against high voltage. For example, if the ADC is measuring high voltage, say the AC line voltage in a metering application, the isolated LVDS buffer requires high working voltage and reinforced isolation.

Figure 2: Isolated LVDS used in a high-voltage motor drive application.

Figure 3: SPI Interface for isolating an ADC from an ASIC.

A third example
A third example as shown in Figure 4 is a generic clock and data-based bi-directional communication between two ASICs, accomplished by two isolated LVDS buffers in 20 configurations.

![Diagram of isolated LVDS communication](image)

**Figure 4: Generic bi-directional clock-and-data communication.**

The isolated LVDS also can be used in applications that traditionally relied upon fiber optic communication - both to provide high throughput and very high voltage-reinforced isolation. These applications include motor drives dealing with system voltages much higher than 1000 V_{RMS}. In the conceptual block diagram shown in Figure 5, several low-voltage (LV) boards (< 1000 V) are stacked together to generate a high-voltage (HV, >> 1000 V) output.

In the traditional approach, a controller communicates with each LV board using fiber optic communication, and the fiber optic link provides reinforced isolation. To reduce system costs, Figure 5 shows an alternative architecture. The controller communicates to one of the LV boards using a fiber optic channel (to provide reinforced isolation). The communication between the LV boards is accomplished by using Isolated LVDS buffers that support 1000 V functional isolation.
The isolation specifications of isolated LVDS buffers depend on the final application and voltages expected across the isolation barrier during operation, including under fault conditions. These requirements can be derived from end-equipment electrical safety standards such as the IEC 61800-5-1 safety standard for AC motor drives, and the IEC 61010-1 safety standard for test and measurement applications.

For example, if using the isolated LVDS buffer for reinforced isolation in a 1000 V\textsubscript{RMS}-rated motor drive application, the isolated LVDS buffer may need to meet a five-second temporary overvoltage specification of 4400 V\textsubscript{RMS}, a surge or impulse voltage of 12 kV\textsubscript{PK}, a working voltage of 1500 V\textsubscript{PK}, and creepage and clearance of at least 14 mm [1]. The Comparative Tracking Index (CTI) of the packaging material used by the IC is also important, which can either limit or enhance the capability of the isolator to handle repetitive or continuous high voltage between the two sides.

If isolated LVDS is being used only for ground loop isolation, then only functional isolation of a few 100V may be sufficient.

The electrical characteristics of the LVDS transmitters and receivers are governed by the TIA/EIA-644-A LVDS standard. Based on this standard the peak differential output on the transmitter pins, when terminated with a 100 Ohm resistor, is around 400 mV. The differential receiver has a sensitivity of 100 mV. The TIA/EIA-644-A standard does not restrict the length of the cable between the transmitter and receiver, but does provide guidelines on how to determine the maximum cable
length for a given data signaling rate. The designer needs to consider the resistive drop, jitter and crosstalk introduced in the cable. Communication over several meters and beyond is possible depending on the data-rates and cable characteristics. Some experimental data is presented in reference [2].

**Isolation in harsh industrial environments**

For isolation applications in harsh industrial environments, immunity to noise and common-mode transients is critical. Using twisted-pair shielded differential cables makes the transmission in the LVDS lines robust against interference. However, the isolation core used in the isolated LVDS buffer must be equally robust as well. Electromagnetic and other disturbances appear as common-mode noise across the isolation barrier. Common-mode transient immunity (CMTI) is a good measure of the robustness of the isolation core.

A key benefit of LVDS signaling is low electromagnetic emissions resulting from differential operation in the transmitter, low output swings, and control over common-mode noise. Again, the isolation core in the isolated LVDS must have very low electromagnetic emissions to preserve this benefit at the system level. Similarly, the isolation core should consume low power even at high data rates in order to maintain the low-power advantage of LVDS signaling.

The maximum supported data-rate, the propagation delay through the isolators, and skew between adjacent channels are important. For motor control applications a data rate of 50 Mbps to 100 Mbps may be required. Low propagation delay is important for SPI applications, and propagation delay skew is important for systems where clock and data are transmitted through two LVDS channels.

**Limitations of existing solutions**

Traditionally high-speed, high-voltage isolation has been accomplished by fiber-optic links, custom designs with high-voltage transformers and capacitors, and a combination of digital isolators with non-isolated LVDS buffers. Fiber-optic links are expensive and difficult to design with. Custom implementations with discrete high-voltage transformers and capacitors take up a lot of board area, have higher power consumption, need careful design for electromagnetic compatibility (EMC) and signal integrity, and are expensive for higher working voltages. Combinations of digital isolators with non-isolated LVDS buffers take up board area, and suffer from signal degradation due to routing between the chips. A fully integrated isolated LVDS buffer provides a low-cost and elegant alternative solution to these approaches.

To address the requirements of the applications as discussed, new isolated LVDS devices are now available in the market. For example, Texas Instruments offers a family of isolated LVDS buffers: ISO7821LL, ISO7821LLS and ISO7820LL. These devices provide data rates up to 150 Mbps, up to 2 kV\textsubscript{RMS}/2828 V\textsubscript{PK} working voltage, 12.8 kV\textsubscript{PK} surge, and 5.7 kV\textsubscript{RMS} withstand voltage. They are available in 8-mm and 14.5-mm creepage and clearance packages that use material group I mold compound
These devices have a minimum CMTI of 100 kV/us, operate from a wide supply voltage range from 2.25 V to 5.5 V, and consume a low current of 10 mA per channel at 150 Mbps. By using isolated LVDS buffers you can provide high-voltage isolation, while establishing a low-cost, low-power, low-emissions, robust communication link over long distance.

References

1. Download the ISO7821LL, ISO7821LLS and ISO7820LL data sheets.

About the Author

Anant Kamath is a systems and applications manager with Texas Instruments where he is responsible for defining new, high-performance analog products as well as application support for existing products in the industrial and automotive markets. Previous roles include a designer and architect of phased-locked loop (PLL) and clock systems, high-speed serializer/deserializer (SerDes), and high-voltage digital isolation devices. Anant has a B.Tech. degree in Electrical Engineering from the Indian Institute of Technology, Madras.

Also see:
- Why isolate LVDS?
- Inexpensive analog isolation using a digital isolator
- Designer's Notebook: Signal Isolation