Xilinx fires a 5G solution shot across the bow of RF and data converter companies

Steve Taranovich - February 21, 2017

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I remember when specialty companies like Graychip made their mark in the '90s with digital down conversion (DDC) and digital up conversion (DUC) ICs along with traditional semiconductor companies that had the high speed op amps and data converters to complete the signal chain in a base station. Digital pre-distortion (DPD) ICs were also used at that time along with the special sauce of an algorithm that improved the distortion of the transmit signal chain. Then, along came the FPGA solutions that upended the traditional market for the DPD and the DUC and DDC solutions. Xilinx had one of those disruptive solutions.

Well, now we are on the road to 5G and fast approaching the need for better signal chain solutions and Xilinx has rocked the industry again. They have embedded RF-class analog technology into their 16nm, all programmable MPSoC architecture. This new RFSoC design does not need discrete external data converters because they have integrated high speed/high performance ADCs and DACs into their SoC solution with a direct RF sampling architecture, bringing the industry closer to the goal of the software defined radio. This added flexibility in the digital domain is great news for 5G with massive MIMO, as well as for millimeter wave wireless backhaul needs. Xilinx claims an amazing board footprint and power savings reduction of 50 to 75%.

Moving from 4G to 5G

Today's 4G radio access networks (RAN) have a bundle of lossy coaxial cables and wires to deal with in order to connect with remote radio heads (RRH). This system has power losses that need to be mitigated (Figure 1).
For many years, designers have been on the ever-elusive quest of moving the digital and analog radios closer and closer to the antenna. The first step toward this goal was using active antenna arrays (Figure 2).
The active antenna array worked for 4G systems, but with the advent of the huge number of connected devices for a viable 5G system, designers needed something new. Along came massive MIMO and beam-forming. These were a good start toward making 5G a reality. The problem that designers needed to solve were the 32, 256 up to 1024 individual antennas needed in a 2D array. This phased-array architecture enables high-resolution beam steering along with lower power consumption. Now high density installations will create much higher density per individual cell (Figure 3).
Figure 3 A massive MIMO 2D array (Image courtesy of Xilinx)

Taking this design to the next level, layouts like mounting “tiles” along the exterior of a building, or billboards/signs, etc. are possible (Figure 4).
**Figure 4** New topologies like antennal tiles along the exterior of a building are leading to ultra-densification. (Image courtesy of Xilinx)

Now here is where the Xilinx all-programmable RFSoC will enable an architecture to leap-frog to the next major step toward realizing 5G—a system design that is scalable for a flexible design with sub-arrays (**Figure 5**).
Figure 5 The Xilinx sub-arrays will enable scalability in a flexible design architecture to fit the particular location. (Image courtesy of Xilinx)

Eliminating the data converter interface and SERDES need

When JESD204B came along to eliminate the messy routing of high speed data converter interfaces, a designer’s task in routing sensitive high speed lines on the PC board was made an order of magnitude simpler. Now taking that effort to the next level, Xilinx has managed to cleverly take routing a step further in simplicity by eliminating existing high-speed data converter interface lines presently running around 12.5Gb/s with the JESD204B protocol and eliminate those PB board lines altogether (Figure 6).
Figure 6 The Xilinx integration of the high speed data converters onto their RFSoC takes the PC board from the top image to the smaller bottom image. This reduces power, board footprint, and speeds a designer’s time-to-market by removing the JESD204B IP cores and serial transceivers from the equation. (Image courtesy of Xilinx)

Let’s just take a look at a typical radio footprint with eight RF DACs and eight RF ADCs and see how the board footprint is reduced by 77% (Figure 7).
How much board space will be saved in multiple sub-array systems of 128×128 transmit/receive design, which 5G systems will need? We are edging closer to miniaturizing 5G systems to a point of realizing true early deployment of a preliminary system at the 2018 Winter Olympics in South Korea and ultimately nearing full deployment reality for the 2020 Tokyo Summer Olympics.

**What will direct RF sampling do for flexibility?**

Conventional intermediate frequency (IF) sampling provides for analog signal conditioning before the ADC. This architecture provides for a pretty power-efficient design, but the multiple analog filter components will have a larger footprint on the PC board, a more complex BOM with bulk analog filter components, and restricted flexibility because of fixed bulk components (Figure 8).
Putting the signal conditioning in the digital domain after the ADC sampling will provide the designer with a greater flexibility in the digital domain, eliminating the higher power, higher sampling, larger board footprint, and BOM complexity of discrete filter components (Figure 9).

Figure 9 Direct RF sampling provides for greater platform flexibility with the choice of having the signal conditioning done in the digital domain after the ADC has done the sampling. (Image courtesy of Xilinx)

Now let’s bring the Xilinx RFSoC into the picture using direct RF sampling and having the signal conditioning after the ADC sampling in the digital domain. This higher integration brings lower power dissipation to the design, smaller footprint, a faster time-to-market with a less-complex BOM, and greater flexibility for the designer by making good use of the digital domain.

The final system design for the radio

By using the TSMC 16nm FinFET advanced CMOS process, Xilinx has created its all programmable RFSoC with integrated digital front-end (DFE), multi-channel scalability needed for 5G, and elimination of the JESD204B bus. This complete RF data converter subsystem on an integrated platform, which I never thought would happen this soon, achieves an amazingly simpler and highly integrated solution, as shown in Figure 10.
As a former RF analog circuit designer who has been with two of the major high speed data converter suppliers, my big question was how did Xilinx get such good performance high speed data converter technology with a 12 bit, 4 Gsps ADC and a 14 bit, 6.4 Gsps DAC?

The answer I discovered was that in 2012 Xilinx designed and validated a 28nm test IC with their Virtex-7 FPGA that had an integrated ADC and DAC. They published those results in a 2014 paper entitled A Heterogeneous 3D-IC Consisting of Two 28nm FPGA Die and 32 Reconfigurable High-Performance Data Converters. They reported the “co-integration of 32 high-performance data converters with high-density digital circuitry in a reconfigurable processing system achieving performance comparable to best-in-class converters.” They published state-of-the-art interface power of only 0.3mW/Gb/s and analog-to-digital die isolation of better than 92dB. Figure 11 shows the architecture of that IC.
My concern here was crosstalk between the multiple DACs and ADCs. In the 2015 paper, it was reported as follows:

- FPGA-to-analog crosstalk was measured by mapping 100 k D-FFs to the FPGA. The D-FFs were simultaneously toggling at the FPGA clock rate while driving 2048 SLLs connected to the 16 DACs. The measurement was done while the DAC synthesized a 70 MHz full scale output tone at 800 MS/s using on-die memory. Measured crosstalk was better than 92 dBc for up to 12 W of switching power.
- The same measurement was performed on the ADC while sampling a 70 MHz input tone at 250 MS/s. The crosstalk was not observable as it was lower than the ADC noise floor.

Pretty darn good. And for performance: Receive SNDR 61.6 dBFS to Nyquist at 500 MS/s and transmit SFDR 63.8 dBc to 400 MHz at 1.6 GS/s was measured. I never thought I would see that in an IC with an FPGA.

They also recently published more results in two IEEE ISSCC 2017 papers: A 13b, 4GS/s Digitally...
Assisted Dynamic 3-Stage Asynchronous Pipelined- SAR ADC and A 330mW 14b, 6.8GS/s Dual-Mode RF DAC in 16nm FinFET Achieving -70.8dBc ACPR in a 20MHz Channel at 5.2GHz, both available here. I took a look at that recent performance in the above 2017 papers and I was again very impressed. See Figure 12 for the ADC results.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>This Work</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (nm)</td>
<td>16</td>
<td>16</td>
<td>65</td>
<td>28</td>
<td>28</td>
</tr>
<tr>
<td>Fs (GS/s)</td>
<td>4.0</td>
<td>4.0</td>
<td>4.0</td>
<td>5.0</td>
<td>5.0</td>
</tr>
<tr>
<td>Interleaving</td>
<td>8x</td>
<td>4x</td>
<td>16x</td>
<td>2x</td>
<td>2x + 8x</td>
</tr>
<tr>
<td>Resolution (bits)</td>
<td>13</td>
<td>13</td>
<td>—</td>
<td>14</td>
<td>10</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>513</td>
<td>300</td>
<td>2200</td>
<td>2300</td>
<td>150</td>
</tr>
<tr>
<td>SNDR (dB) @ peak</td>
<td>63.8</td>
<td>60.0</td>
<td>61.0</td>
<td>63.0</td>
<td>57.0</td>
</tr>
<tr>
<td>SNDR (dB) @ Nyq.</td>
<td>57.3</td>
<td>56.0</td>
<td>55.5</td>
<td>58.0</td>
<td>52.2</td>
</tr>
<tr>
<td>SFDR (dB) @ Nyq.</td>
<td>67.0</td>
<td>68.0</td>
<td>64.0</td>
<td>70.0</td>
<td>58.5</td>
</tr>
<tr>
<td>FoMValden @ Nyq. (fJ/conv-step)</td>
<td>214.2</td>
<td>145.5</td>
<td>1130.0</td>
<td>708.7</td>
<td>90.1</td>
</tr>
<tr>
<td>FoMSchaefer @ Nyq. (dB)</td>
<td>153.2</td>
<td>154.2</td>
<td>145.1</td>
<td>148.4</td>
<td>154.4</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>1.04</td>
<td>0.34</td>
<td>12.0</td>
<td>14.4</td>
<td>0.45</td>
</tr>
</tbody>
</table>

**Figure 12** The latest performance summary of the ADC and a comparison to prior works—see below for the titles of those four efforts (Image courtesy IEEE ISSCC 2017)

The four references called out in Figure 12:


And now for the DAC results in Figure 13:
The references called out in Figure 13:


So TSMC’s 16nm FinFET process and Xilinx clever designers have combined to show exceptional high speed analog results, especially in the performance/watt of the converter subsystems in the RFSoC. The IC is using a **ZYNC Ultrascale+ MPSoC** 64 bit processor scalability. Xilinx claims that this IC will apply Moore’s Law to analog. I agree. Let’s see how the 2018 and 2020 Olympics deploy some of this technology to realize 5G promises.

Right now the 16mm test chip is on an evaluation board and will begin moving to the production phase for product launch target later this year. This solution will be supported by the Xilinx **Vivado High-Level Synthesis tool**.

**Also see:**

- [Millimeter wave wireless for 5G](#)
- [5G: What to expect](#)
- [5G: The race is picking up pace](#)
- [Where RF meets analog and digital—the new embedded reality](#)
- [Torture-testing your new SoC’s security quotient](#)