Introducing RFSoC

Rajan Bedi - March 14, 2017

Several of my ground-segment clients and I are considering Xilinx's recently announced RFSoC for future transceivers, so it would be timely to introduce the benefits of this impending device.

Direct RF/IF sampling and direct DAC up-conversion are being used very successfully in-orbit and on the ground, e.g. bandpass sampling provides flexible RF frequency planning with some spacecraft directly digitising L and S-band carriers to remove expensive and cumbersome superheterodyne down-conversion stages. Today, many navigation satellites directly re-construct the L-band carrier from baseband data without using traditional up-conversion. Direct RF/IF sampling and direct DAC up-conversion have dramatically reduced the BOM, size, weight, power consumption, and the non-recurrent and recurring cost of transponders. Software-defined radio has given operators real scalability, reusability, and reconfigurability, and Xilinx's new RFSoC will offer further hardware integration advantages for the ground segment.

RFSoC integrates GSPS ADCs and DACs with a Zynq UltraScale+ MPSoC all of which have been fabricated using 16 nm FinFET CMOS. At this geometry and with this technology, the mixed-signal convertors are very low power and economies of scale have made it possible to add a lot of digital post-processing (Moore digital - small A/big D!) to implement functions such as DDC, DUC, AGC, and interleaving calibration.

While CMOS scaling has improved the speed of ADCs/DACs, which has resulted in larger bandwidths at lower power, for analogue designs, the transconductance of transistors and the size of the analogue input/output voltage swing have reduced. The latter, for example, impacts G/T at the satellite receiver.

Integrating ADCs and DACs with Xilinx's programmable MPSoC fabric reduces physical footprint and chip-to-chip latency, and completely eliminates the external digital interfaces between the mixed-signal convertors and FPGA which are typically power consuming, large, and difficult to route for parallel I/O.

There will be a number of devices in the RFSoC family each containing different ADC/DAC combinations targeting different markets. Depending on the number of integrated mixed-signal convertors, Xilinx is predicting a 55 to 77% reduction in footprint compared to current discrete implementations using JESD204B high-speed serial links between the FPGA and the ADCs/DACs as illustrated below. Integration will also benefit clock distribution both at device and system level.
The integrated 12-bit ADCs can each sample up to 4 GSPS which offers flexible bandwidth and RF frequency planning options. The analogue input bandwidth of each ADC appears to 4 GHz which allows direct RF/IF sampling up to S-band.

Direct RF/IF sampling obeys the bandpass Nyquist Theorem when oversampling at least twice the information bandwidth and undersampling the absolute carrier frequencies. For example, the spectrum below shows a 48.5 MHz, L-band signal centred at 1.65 GHz digitised using an undersampling rate of 140.5 MSPS. The resulting oversampling ratio is 2.9 with the information located in the 24th Nyquist zone. Digitisation aliases the bandpass information to the first Nyquist zone which may or may not be baseband for you depending on your application. If not, RFSoC's integrated DDC moves the alias to dc allowing the use of a low-pass filter.
As the sampling rate increases, the noise spectral density spreads across a wider Nyquist region with respect to the original signal bandwidth, e.g. each time the sampling frequency doubles, the noise spectral density decreases by 3 dB as it re-distributes across twice the bandwidth which increases dynamic range and SNR. Understandably, operators want to avail of this processing gain! A larger oversampling ratio also moves the aliases further apart relaxing the specification of the anti-aliasing filter. Furthermore, oversampling increases the correlation between successive samples in the time-domain, allowing the use of a decimating filter to remove some and reduce the interface rate between the ADC and the FPGA.

The integrated 14-bit DACs can each sample up to 6.4 GSPS which offers flexible bandwidth and RF frequency planning options. The DACs have a mixing micro-architecture and use DUC to place the carrier information in Nyquist zones 1, 2 and 3 - up to the end of C-band.

Just like any high-frequency, large bandwidth mixed-signal device, designing-in RFSoC requires careful consideration of floor-planning, front/back-end component placement, routing, grounding, and analogue-digital segregation to achieve the required performance. The partitioning starts at the die and extends to module/sub-system level with all the analogue signals (including the sampling clock) typically on one side of an ADC/DAC. Given RFSoC's frequencies, at a PCB level, analogue inputs and outputs must be isolated further to prevent crosstalk between neighbouring channels, clocks, and digital noise.

At low carrier frequencies, the performance of an ADC/DAC is limited by its resolution and linearity (DNL/INL), however, at higher signal frequencies, SNR is determined primarily by the purity of the sampling clock. For direct RF/IF applications, minimising jitter will be key to achieving the desired performance as shown below.
While there are aspects of the mixed-signal processing which could be improved, from the early announcements and information posted on their website, Xilinx has done a good job with RFSoC. Although not specifically designed for satellite communication, more so for 5G MIMO and wireless backhaul, RFSoC's ADCs and DACs have sufficient dynamic range and offer flexible RF frequency planning options for many ground-segment OEMs. First samples will become available in 2018 and I look forward to designing-in the part and sharing my experiences with you.

Until next month, happy sampling! The first person to tell me why the orientation of the alias in the first Nyquist zone differs to its bandpass carrier in Figure 2 will win a Courses for Rocket Scientists World Tour tee-shirt. Congratulations to Abhishek, a power engineer from India, the first to answer the riddle from my previous post.

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