A self-calibrating low-power 16-bit 460 kS/s SAR ADC for microcontroller applications

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I. Introduction

Low cost microcontrollers are increasingly expected to provide high performance analog functions for applications that previously used stand-alone ADCs. These applications include power metering, handheld medical devices, industrial control systems, power management systems, gaming consoles, and instrumentation. For use in a generalized control system, the low latency and high bandwidth of a Nyquist ADC is required but with accuracy around 14 effective number of bits (14-bits ENOB), low power, and cost that makes the device reasonable for mass-market. This combination of requirements makes most available SAR and Sigma-Delta (DS) ADCs ineffective because the cost and power targets are difficult to achieve in combination with the frequency and latency requirements. This paper describes a low power 16-bit SAR ADC based on a self-calibrating, self-testing architecture with a double-bridged split CDAC and a high speed three-stage comparator. This architecture has been demonstrated in production to achieve up to 14.5 ENOB at a total cost (implementation and test) significantly lower than most mass-market 12b SAR ADCs.

As the resolution of the SAR ADCs increases, the number of CDAC unit elements increases linearly, but matching requirements of those elements cause a square law area increase. In order to limit the total number of elements, bridging or scaling elements are commonly used to split the DAC into smaller sub-DACs. These scaling elements are non-unit size and have associated parasitics that can cause further mismatch and errors. In general, matching beyond 10-11 bits is not feasible [1][2] for microcontroller integration due to area constraints. Therefore some form of calibration of the ADC DAC elements is necessary to meet the higher resolution and accuracy requirements. In this paper the design of a differential, area efficient 16-bit self-calibrating SAR ADC is presented. The ADC architecture is described in section II. The CDACs are described in Section III. Section IV gives a brief description of the calibration. Section V depicts the high-speed comparator, and then silicon results are described in Section VI, followed by conclusions in Section VII.
Figure 1 Fully differential ADC Architecture with 2 complementary CDACs.

II. ADC Architecture

Figure 1 shows the ADC architecture, not including the channel multiplexors. SAR ADCs typically consist of a DAC and a comparator in a feedback loop with logic including a successive-approximation register. The DAC typically consists of an array of binary weighted elements, in our case capacitors. In some applications, it is desirable to be able to convert a differential input signal where the polarity of the differential input is unknown. Converting a differential signal also helps increase the accuracy of the result due in part to common-mode noise rejection.

One of the limiting factors in implementing a differential ADC is keeping the comparator’s inputs within its common mode range during successive approximation. When a comparator is auto-zeroed at a common mode voltage, moving its inputs away from that common mode voltage will cause errors in the conversion result which results in increased non-linearity. To prevent this problem, we include a smaller, lower-power “non-critical” comparator. A partial successive approximation is done using this comparator and the minus side DAC, which samples Vin-. This gets the comparator minus input V- close enough to Vcm for the comparator to be accurate within 1 LSB. The number of approximations required on the minus side is dictated by the common mode rejection ratio (CMRR) of the comparator and the resolution of the ADC. The higher the CMRR of the comparator, the fewer approximations required. For example, a comparator with 66 dB of CMRR in a 12-bit ADC only requires 2 approximations on the minus side (1/2 of 12-bits LSB = 78 dB, so minus approximation needs to reduce the |Vcm-V-| voltage by 12dB).

Our implementation is a 16b ADC (1/2 LSB = 102 dB) with a comparator CMRR of about 72 dB. Therefore, we require 5 approximations (25 = 30 dB). For a 5-bit SAR the smallest input voltage the “non-critical” comparator must resolve is VREFH/32. After the partial successive approximation on the minus side, a full 16 step approximation is done using the accurate comparator and the plus side DAC, which samples Vin+. Both comparator outputs are captured by the SAR logic to control the
respective DACs in order to do the successive approximation. The uncalibrated result is determined by subtracting the minus side result from the plus side result. A pre-determined calibration value is then subtracted from the uncalibrated result to give the final conversion result. This differential mode can run at up to 320 kS/s. A single-ended mode is also available. It does not require the partial successive approximation on the minus side and can therefore run up to 460 kS/s. The ADC also has a lower resolution 12-bit mode that can run up to 1 MS/s.

CDAC arrays

III. CDAC arrays

The CDAC is the most critical component of the SAR. The linearity of the SAR ADC is dependent upon the capacitor matching in the capacitor array. A split-capacitor structure is common to limit silicon area [6][7]. The CDAC topology illustrated in Figure 2 when combined with calibration provides an optimal design trade-off among capacitor array size (96 capacitors), speed, noise, and linearity. Each capacitor represents an array of unit capacitors. The calibration of the most significant capacitors allows smaller sizing of the unit capacitor. In this design a unit fringe capacitor of about 125fF is used to provide sufficient matching for the uncalibrated capacitors and to keep $kT/C$ noise below 1 LSB at 16 bits. The CDAC is partitioned into 3 binary weighted sub-DACs based on unit size capacitors. The most-significant-bit (MSB) sub-DAC contains 5 bits, the intermediate (ISB) sub-DAC contains 5 bits, and the least-significant-bit (LSB) section contains 6 bits. The LSB section is built as a 5 bit array with a half-sized capacitor for the bit 0 and termination.

![Figure 2](image)

**Figure 2** Fully differential 5b-5b-6b split CDAC topology with 2 bridging capacitors.

IV. ADC Calibration

There are many methods of calibration for SAR ADCs. Some methods use digital correlation-based
calibration [8][9][10]. Other methods use a technique to measure differences in capacitance ratios in the DAC [3] and then use analog adjustments to modify DAC elements [6][7] or digital adjustments to adjust the result [4][5]. This ADC uses a measurement method similar to [3] that measures differences in capacitor ratios to determine capacitor error values and then make digital adjustments to modify the result similar to [4][5]. Each of the MSB capacitors on both the plus and minus side CDACs are calibrated. In order to be able to adjust the SAR result without creating large non-linearities, the uncalibrated CDAC must be monotonic. In order to guarantee monotonicity we size the scaling capacitor Csc1 (see Figure 3) slightly larger than ideal. **Figure 3** illustrates this concept.

To determine calibration error values, each MSB capacitor (controlled by bits15:11) is compared against the combination of all lower significance capacitors. For example, one step of the calibration would be to compare the bit 11 capacitor (1C) to bit 10:0 capacitors plus termination capacitor (slightly larger than 1C due to oversizing of Csc1). The next step would be to compare the bit 12 capacitor (2C) to the bit 11:0 capacitors plus the termination capacitor (slightly larger than 2C). This process is repeated for each of the MSB capacitors. The calibration coefficients are accumulated and stored in memory and require less than 128 bits per ADC. After a normal ADC conversion the calibration value corresponding to the MSB result is subtracted from the uncalibrated result to obtain a calibrated result.

A gain factor based on the accumulated calibration coefficients is then applied to produce the final conversion result. This calibration method compensates for mismatch amongst the MSB capacitors and also mismatch and parasitics of the first scaling cap. It is important to point out that, in order to improve linearity and tolerate process gradients on the uncalibrated capacitors and to limit the calibration ranges, common-centroid layout techniques must be utilized. A dummy capacitor ring was also adopted on the edges of the capacitor array to ensure that all unit capacitors in the capacitor array have the same structure around them.

![Non linearities due to capacitor mismatch in a standard binary-weighted DAC](image1)

![Non linearities due to capacitor mismatch in a binary-weighted DAC with oversized first scaling capacitor](image2)

![No non-monotonicities, High linearity](image3)

**Figure 3** Non-linearities and proposed method to improve CDAC linearity.
Table 1 Monte Carlo simulation of CDAC INL and DNL, typical and worst case results.

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<th>DNL</th>
<th>INL</th>
<th>ENOB</th>
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<td>+41.7</td>
<td>-22.1</td>
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<tr>
<td>Calibrated</td>
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<td>+1.40</td>
<td>-1.57</td>
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<th></th>
<th>DNL</th>
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<tbody>
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<td>Calibrated</td>
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<td>+0.96</td>
<td>-0.18</td>
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Comparator design

V. Comparator design

![Comparator design diagram]

Figure 4 Fully differential comparator with capacitive coupling and autozero

The primary comparator design tradeoff is speed vs. accuracy. The accuracy is achieved by providing sufficiently high gain, low offset, and low input referred noise. Comparator offset translates into offset in the ADC transfer characteristic, but does not affect ADC linearity. In our implementation, the offset is canceled by means of auto-zeroing techniques. The comparator needs enough gain to resolve a voltage smaller than 1 LSB, as low ~15 mV in 16-bit mode, and provide a response within the required delay time. With a maximum ADC clock of 12 MHz in 16-bit mode, the
comparator is given approximately half of one period, or 41.6 ns, to complete each comparison.

A three-stage comparator was chosen as tradeoff between speed and gain. Each stage is auto-zeroed independently and capacitively coupled to the next stage. Note the first 2 stages are fully differential comparators while the third one is a single ended stage. **Figure 5** shows a simplified schematic of the comparator stages. A folded cascode structure is used to provide enough gain to resolve voltage levels associated with a 16-bit ADC. During the ADC sampling/auto-zero phase, the gates of differential pair M1-M2 are connected to the analog ground voltage (cazd high), while the output stage is configured for low-gain by M13 - M14 (casz high) in order to store offset on C3 and C4.

**Figure 5** Min/Max INL in LSB's vs. reference voltage, temperature and sampling frequency in 16-bit differential mode at maximum conversion rate.

At the end of the auto-zero phase, first casz is deasserted and then cazd is deasserted using non-overlapping clock phases. The ADC then begins the successive approximation phase, the comparator stage is switched to a high gain configuration and the input signal is amplified by the folded cascoded gain stage. During successive approximation cycles, the DAC is allowed to settle (clk high) while the comparator output stage is reset by M12. Next, clk is deasserted and the comparison is made. Comparator layout critical to the performance of the ADC, and special care is required to prevent coupling of analog and digital signals.

**VI. Experimental Results**

The ADC was fabricated in a 90-nm bulk CMOS process. The ADC circuit has been integrated on 90nm microcontroller families, and is currently in production. **Figure 5** shows ADC Integral Non-Linearity (INL) measured on 4 random devices from a production wafer lot. It shows minimum and
maximum INL at maximum conversion rate with clock frequencies from 1 MHz to 12 MHz (maximum clock rate), voltages from 1.71 V to 3.6 V and temperature variation from -40°C to 125°C.

**Figure 6** shows the ENOB at 8 MHz and 12 MHz clock rate, achieving almost 15-bits ENOB at a conversion rate 11 kS/s.

![Figure 6](image)

**Figure 6** SAR ADC ENOB vs sampling frequency in typical conditions.

**Figure 7** shows a snapshot of the ADCs on the microcontroller die. The CDACs are located in the central portion of the layout whereas the switches are underneath each fringe capacitor unit. The comparators and current reference are below the CDACs, and channel multiplexers are above the CDAC, on the top side of the circuit.
VII. Conclusions

A low power differential self-calibrating 460 kS/s 16-bit rail-rail-input SAR A/D converter has been implemented in a 90-nm bulk CMOS technology using metal fringe capacitors. With a measured current dissipation of 800 mA at full speed, this ADC is suited for many applications. Silicon measurements show an overall performance of 13.5-14.5 ENOB. The circuit has been integrated on 90 nm microcontroller families and actively in production.

VIII. Acknowledgments

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IX. References

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