Ultra deep-submicron FPGAs and broadband ADCs/DACs are increasingly being used by high-throughput satellites exploiting the on-board processing and flexibility advantages of digital payloads. Wideband mixed-signal converters now directly digitise/re-construct IF/RF carriers to remove superheterodyne frequency-conversion stages to make transponders smaller, lighter, less power consuming, and more affordable.

When sampling low-frequency or baseband signals, the performance of an ADC/DAC is limited by its resolution and linearity (DNL/INL). However, for bandpass IF/RF carriers, SNR is determined by the purity of the sampling clock. For direct RF/IF applications, minimising phase noise (jitter) is key to achieving the desired performance. Higher input frequencies (and amplitudes) have increased slope (slew rate), reducing the conversion error caused by timing jitter as shown below.

As an example, many high-throughput payloads are currently processing information bandwidths of 500 MHz centred at L or S-band using 10 or 12-bit ADCs/DACs. Figure 2 shows that with 0.5 ps rms of sampling-clock jitter (dashed lines), the SNR achievable by directly processing IF/RF carriers between 1 and 4 GHz has dropped well below the expected performance for each resolution. With 17 fs rms of jitter on the clock (solid lines), the resultant SNR is acceptable to satellite operators.
Figure 2 SNR of an ideal ADC vs. analogue input frequency and clock jitter

In addition to the intrinsic impurity of an oscillator, there are many sources of external jitter which increase the total phase noise seen at the ADC/DAC clock input, e.g. crosstalk, EMI, ground effects, and supply noise. However, jitter only affects ADC/DAC performance during the transition or threshold of the sampling clock as illustrated in Figure 1. Making the sampling-clock edge faster by increasing its slew rate reduces the amount of time noise is present during the switching threshold. Increasing either frequency or amplitude increases the slope of the clock to mitigate the effects of jitter.

As the sampling rate increases, the noise spectral density spreads across a wider Nyquist region with respect to the original signal bandwidth; each time the sampling frequency doubles, the noise spectral density decreases by 3 dB as it re-distributes across twice the bandwidth increasing dynamic range and SNR. Understandably, operators of high-throughput satellites want to avail of this processing gain! A larger oversampling ratio also moves the aliases further apart relaxing the specification of the anti-aliasing/imaging filter.

Increasing the amplitude of the sampling clock also increases its slew rate minimising the effects of jitter. Designers tend to clock IF/RF ADCs/DACs at their typical clock amplitude, between +1 and +3 dBm. However, most broadband space-grade ADCs/DACs will accept clock powers up to +7 or +10 dBm. The output power from Q-Tech's QT725S SAW oscillator can be specified up to +10 dBm (±1.5 dB) to maximise the performance from IF/RF ADCs/DACs. Diodes can also be placed at the ADC/DAC’s clock input to exploit the slew rate advantages of higher amplitudes while ensuring a compatible level.

A SAW resonator is a high-Q quartz device which enables the QT725S to achieve an ultra-low phase jitter of 17 fs rms up to 1.6 GHz from −40 to +85°C, allowing it to clock IF/RF ADCs/DACs to deliver maximum SNR. Its low inherent phase noise avoids the need for an external narrow-band filter reducing the BOM, component costs, and PCB area.
Figure 3 Q-Tech's, space-grade, hermetic, voltage-controlled SAW oscillator

The ultra deep-submicron FPGAs used within the latest high-throughput satellites are exploiting high-speed serial links for intra-payload communication. SERDES requires a dedicated crystal oscillator to generate a reference clock with fast rise and fall times, typically 200 ps (20%-80%), to minimise the effects of jitter on the link margin.

A recent innovation is a four-point mount crystal oscillator (XO) which increases rigidity without requiring additional PCB area for high-shock and high-reliability applications. A small form factor and low mass offer extra protection from shock and vibration, and a part has been qualified to 20,000 g. The QT186 XO has been placed in a 5×7 mm hermetically-sealed package, is available in surface-mount, through-hole, or leaded, and weighs 0.6 to 3 g. The device is powered using a single voltage from 2.5 to 5V and can be ordered from 1 to 162.5 MHz with CMOS, LVDS, or LVPECL outputs. The qualified part operates from −55 to +125°C and has specified latch-up and total-dose tolerances of 75 MeV-cm$^2$/mg and 100 kRad(Si) respectively. The typical (20%-80%) rise/fall time for the LVPECL part is 300 ps.

Figure 4 Four-point mount, space-grade crystal oscillator

Many high-throughput payloads need to distribute multiple identical clocks to many devices. The QT625x range of XOs outputs between 2-12 LVDS clocks ranging from 15 to 200 MHz with a maximum skew of 400 ps between these. The phase jitter integrated from 12 kHz to 20 MHz is less than 1 ps rms.
Young engineers are mesmerised by the latest FPGAs and ADC/DACs, however, these need to be powered and clocked properly to deliver their specified performance. Such parts have unique clocking requirements and the solutions discussed will enable the next generation of high-throughput satellites. It's important that external sources of jitter from the clock or power distribution do not compromise the intrinsic purity of the oscillator and I teach how to design-in and what to avoid on my Mixed-Signal and FPGA training courses.

The Q-Tech and Wavelength oscillators presented undergo the standard screening for MIL-PRF-38534 and MIL-PRF-55310 (qualifies to MIL-STD-790) for Class B/H and Class S/K parts. Complete lot testing includes checks for electrical, frequency-temperature stability, frequency-voltage tolerance, overvoltage survivability, visual, mechanical, solderability, and aging. Tests performed on a sample include vibration, shock, ambient pressure, thermal shock, storage temperature, resistance to soldering heat, moisture resistance, salt spray, terminal strength, resistance to solvents, and radiation testing.

Until next month, happy clocking! The first person to tell me how to convert phase noise to jitter will win a Courses for Rocket Scientists World Tour tee-shirt. Congratulations to Andreas, a systems-engineer from Germany, the first to answer the riddle from my previous post.

Also see:

- Wideband testing of satellites
- Jitter and the ins and outs of SNR
- Oscillators: How to generate a precise clock source
- Spread-spectrum clocking reduces EMI in embedded systems
- Rule of Thumb #2: Signal bandwidth from clock frequency
- Spread-spectrum clocking in PCI Express