



[PAM4, error correction bring 400GbE test challenges](#)

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Earlier this year, IEEE802.3bs compliant, line rate 400 Gigabit Ethernet (400GbE) traffic via four-level Pulse Amplitude Modulation (PAM4) electrical lanes was [successfully demonstrated](#) for the first time at OFC 2017 in Los Angeles—proving that the higher-speed Ethernet ecosystem is here. Growing bandwidth requirements from increasing cloud adoption is making 400GbE and the faster networking speeds it entails an essential milestone in the drive toward true terabit Ethernet.

What's different?

400GbE is the first Ethernet speed in which the IEEE standards governing body includes [Forward Error Correction](#) (FEC) as a hard requirement in all use cases. FEC is needed with the inclusion because of the PAM4-based electrical interface (**Figure 1**). Once FEC is required for one interface, it became a requirement for all. Before 400GbE becomes a reality, companies in the ecosystem need to test the technologies behind it. We can no longer use yesterday's procedures; the testing infrastructure must account for the inclusion of FEC.

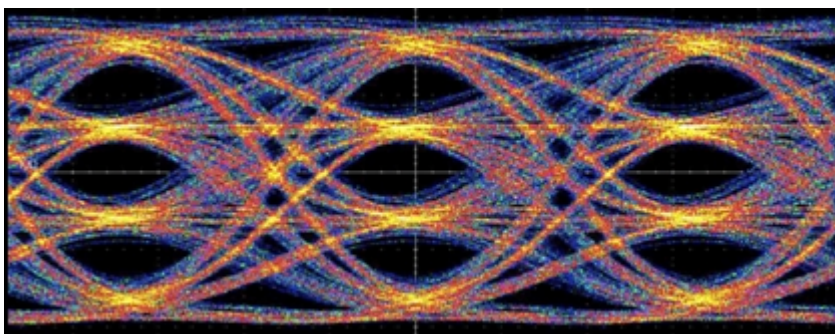


Figure 1. A PAM4 modulated signal has four amplitude levels and three eyes.

FEC has traditionally been used in networking standards such as Synchronous Optical Networking (SONET) and Optical Transport Network (OTN), which use stronger FEC than the one called out in IEEE 400 GbE. FEC was introduced into 10GbE and 100GbE initially for backplane uses—then for a few of the front-panel use cases, such as copper cabling, to deliver a more economical technology.

[See: [PAM4: A new measurement science](#)]

The IEEE is allowing a higher acceptable bit-error rate (BER) on the optical interfaces pre-FEC, and KP4 FEC is used to correct incoming errors up to a specified threshold. (Without FEC, BER levels are typically 10^{-12} and 10^{-13} .) Therefore, FEC is used to correct up to an IEEE defined error level

of 15 symbol errors per code word. Beyond that level, [KP4 FEC](#) no longer can correct incoming errors. IEEE requires FEC for all front panel use cases for 400 GE.

[See: [Don't confuse PAM4 SER and BER](#)]

Led by the needs of cloud-scale data centers, FEC enables the ecosystem to have lower performance specifications of electrical and optical components for a given [physical medium dependent](#) (PMD). Essentially, FEC reduces power and cost.

Implications of FEC on testing protocols

Traditionally, tests see a lack of errors as "good" or "passing" and the presence of errors as "bad" or "failing." With 400 GbE, naturally occurring errors in the system are "acceptable" to a certain level and then corrected with FEC, resulting in a nearly error-free environment post-FEC. With 400GbE, post-FEC BER could be misleading because FEC corrected the incoming errors. To ensure proper operations, visibility into the error density and distribution is essential to determine the health of the system. A simple analogy would be driving at high speed close to a cliff. You would want to know how close or far you are from the edge.

Hardware manufacturers will need to change their testing procedures to take this into account, and use different metrics to test link performance and compliance. As an example, previously, when there were no errors at the packet level, there would be no need to review the [Physical Coding Sublayer](#) (PCS) lanes or physical lanes for errors. Now, even with acceptable post FEC BER, a new procedure is required to see the mapping of corrected bits back to the same PCS or physical lanes. If a particular lane has significantly higher error density than others, it's cause for concern even though the post-FEC BER is acceptable. All 8x50 Gbps lanes are no longer equal in terms of BER.

Previously, the presence of any errors would be unacceptable. Now, with FEC, insight into symbol errors distribution post FEC is critical to determine the health of the system, i.e. how close or how far it is to the uncorrectable threshold specified by the IEEE standards.

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