Realizing 5G New Radio massive MIMO systems

Paul Newson, Hemang Parekh, Harpinder Matharu, - January 08, 2018

Massive MIMO, which depends on using a large array of antennas, is the keystone technology for realizing the improvement necessary to justify the evolution from 4G to 5G wireless networks.

Fifth generation (5G) wireless access networks are being defined to meet the perpetual growth in demand for capacity and address new use cases and applications in 2020 and beyond. 5G New Radio (NR) targets up to 10Gbps peak data rates per user to offer enhanced mobile broadband (eMBB) services, which represents roughly 100× improvement over 4G networks.

Massive MIMO is a primary means of accomplishing this. The technology is particularly well suited for underutilized TDD (time division duplex) bands below 6 GHz, such as band 40 (2.3 GHz), band 41 (2.5 GHz), band 42 (3.5 GHz), and band 43 (3.7 GHz), many of the unlicensed bands set aside for wireless communications, along with other bands that will be newly allocated for commercial wireless networks.

Massive MIMO is important for enabling dynamic digital beamforming to implement user-by-user beams to theoretically offer full cell capacity to each user, which otherwise is shared amongst users on a time and frequency basis. There is no change required in the existing user equipment to benefit from massive-MIMO-enabled cell towers.

The promise of massive MIMO is so appealing that many of the operators do not want to wait for the completion of 5G NR standards and are considering its deployment on 4G equipment. However, these benefits come with a set of challenges.

The larger footprint and higher power and cost due to multifold increase in system complexity in implementing massive MIMO radios is a major hurdle. Overcoming the challenges will require the integration of the analog signal chain with digital front end (DFE) devices in the radio, along with substantial increase in the signal processing compute power.

Massive MIMO and beamforming

Beamforming is not a new concept and has been around in the cellular market as active antenna systems (AAS) that use static beamforming in the radio as a tradeoff to contain the system cost and complexity. AAS are applicable in coverage limited networks, but today’s congested networks need dynamic digital beamforming to get the maximum possible spectral efficiency improvements.

Massive MIMO with full digital beamforming adds a spatial dimension to frequency and time dimensions to significantly boost spectral efficiency. The resulting SNR (signal to noise ratio) improvements brought about by the array gain and orthogonality of multiple beams means the same time and frequency allocations can be reused by multiple users.
Massive MIMO system: Base station dis-aggregation and functional partitioning

The complexity associated with the massive MIMO architecture mandates a significant design alteration: the disaggregation of the base station to support new functional partitions to manage in-system connectivity bandwidth.

For example, in a 100 MHz 64T64R (transmit/receive) antenna array system, the bandwidth between baseband and radio functions is 230 Gbps, assuming that the baseband and radio functions are implemented using one device each. In reality, systems use multiple devices to implement either 8T8R or 16T16R array DFE radio function modules resulting in more than doubling in-system connectivity bandwidth requirements.

Figure 2 provides a conceptual diagram of a massive MIMO radio system. Digital radio processing blocks implement 8T8R or 16T16R DFE functions with integrated analog to digital converters (ADCs) and digital to analog converters (DACs). This is a must-have to eliminate the JESD204B connectivity links ordinarily required for interfacing digital and analog domains; their elimination will help to lower system footprint, power, and cost.
The beamforming device brings Layer 1 baseband functionality to radio to substantially reduce connectivity bandwidth requirements with the higher-layer baseband functions that can now potentially be virtualized in the mobile edge. Integration, flexibility, and higher compute power are three critical requirements to optimally implement massive MIMO systems and evolve associated beamforming and DFE algorithms to continually improve performance, cost, and power.

Programmable RFSoCs
A 5G NR massive MIMO implementation requires a large number of active signal chains in the radio to connect to each antenna or subset of antennas in the array. These active signal chains, which traditionally comprise data converters, filters, mixers, power amplifier, and low noise amplifier, can lead to significant increase in power, form factor, and cost of the system. The large number of active signal chains in massive MIMO systems increase in system power and footprint, making it difficult to realize commercially viable systems. The costs associated with moving data between the RF front-ends (RFFE) and the DFE is one of the key challenges that must be resolved in 5G; the issue must be addressed at the software, hardware, and system levels.

In order to address this challenge, Xilinx has replaced multiple ADCs and DACs along with many other RF components on the board by integrating direct RF-sampling data converters into the existing 16nm FinFET multi-processing SoC (MPSoC) family of products designed and deployed for radio applications. This new SoC device family, called “All Programmable RFSoC,” monolithically integrates RF sampling data converter technology to provide a fully hardware and software programmable wide bandwidth platform for radio systems.

Based on an ARM-class processing subsystem merged with FPGA programmable logic, the architecture features 12-bit, 4GSPS (gigasamples per second) RF-sampling ADCs, and 14-bit, 6.4GSPS direct RF DACs, along with optimized digital down-conversion and up-conversion signal processing.

Moving RF into the digital domain by integrating RF-sampling data converter technology not only overcomes power, space, and cost disadvantages but enables implementation of wide bandwidth and multi-band systems.

Figure 2 Conceptual massive MIMO architecture
Analog RF in existing radio systems is typically designed to relax discrete data converter specifications. In addition, discrete data converters and analog RF components use older process nodes and are typically optimized for narrow bandwidths. This results in analog RF solutions that are expensive in size, power, and cost for wide bandwidth MIMO and massive MIMO radio systems. Integrating high speed data converters, 6.4GSPS direct RF DACs and 4GSPS RF-sampling ADCs, allows digital RF to be flexible, low power, and wide bandwidth, ideally suited for building MIMO and massive MIMO systems with lower footprint, power, and cost.

16nm FinFET technology

The monolithic integration of high speed RF components benefits from the excellent analog transistor characteristics that can be wrung out of the 16nm FinFET process. The ON resistance of the transistor is extremely low, which allows implementation of wide bandwidth RF sampling signal switches with high precision. In turn this enables the integration of cost-efficient and power-efficient high speed comparators, amplifiers, clocking circuits, and digitally-assisted analog calibration logic, all with excellent characteristics.

The digital implementation in 16nm FinFET versus 65nm (typically used for analog RF components) results in more than 10× area reduction and 4× power reduction. Xilinx has innovated ideal design solutions to implement power integrity, digital calibration loops for high precision, and robust isolation strategies.

The digital-RF resources integrated in RFSoC are comprised of multiple channels of 6.4 GSPS DACs and 4 GSPS ADCs, integrated low phase noise PLLs and full complex mixers – 48-bit numerically controlled oscillators (NCO) for each DAC and ADC. The RF data converter arrays come with 1×, 2×, 4×, 8× interpolation and decimation filters and implement flexible FPGA fabric interface. In addition, the direct RF-DAC block implements quadrature modulation correction (QMC) and Sin x/x (Sinc) correction filters.

Massive MIMO in RFSoC

Figure 4 illustrates a typical massive MIMO radio implementation using one of the RFSoC devices. The RFSoC has 33 Gbps transceivers with hardened 100G Ethernet MAC/PCS with an RS-FEC that can be leveraged depending on the flavor of fronthaul interface, be it 25G CPRI or the eCPRI.
Partial L1 functionality, such as iFFT/FFT transforms and associated physical random access channel processing, can be moved to the radio for 50% bandwidth reduction (and cost & power savings) between radio and baseband unit.

RFSoC devices provide rich high performance low power DSP resources to implement a digital front end comprising digital up conversion, crest factor reduction, digital pre-distortion, passive intermodulation correction, equalization, and down conversion.

Appropriate interpolation filters on the transmit path and decimation filters on the receive path are used to run RF-DAC and RF-ADC at high clock frequencies, independent of the FPGA fabric frequencies, for better frequency planning. With careful frequency planning, multiple bands, such as band 1 and band 3 for FDD massive MIMO and band 38, 40, 41 and bands 42 and 43 for TDD massive MIMO, can be simultaneously supported leveraging the wide bandwidth of the integrated RF signal chain.

RFSoC has quad-core ARM Cortex-A53 multiprocessor cores running up to 1.5 GHz along with dual-core real time ARM Cortex-R5 multiprocessor cores running at 533 MHz. This is significant compute resource for computing pre-distortion coefficients and performing system control, RF calibration, and general operation and maintenance functions.

The programmable logic coupled with on chip compute can be used to support open source APIs to future-proof the radio system for software defined networking where radios can be configured dynamically based on the customer demand. Machine learning algorithms can be efficiently implemented in the fabric to automate management of increasing numbers of fragmented spectrum bands, spectrum sharing, and hosting mobile virtual network operators (MVNO).

To enable integration, Xilinx provides a library of state of the art DFE IP for CFR (crest factor reduction) and DPD (digital pre-distortion) along with DFE subsystem reference design and DFE demonstration kits for 4G, LTE-Pro, and 5G applications.

In order to demonstrate system performance on an RFSoC, the ZU28DR device based RFSoC characterization board is connected to a Xilinx RF front end card with two transmit and two
multiplexed receive paths to support PA feedback as well (Figure 5). With this board setup, and connecting a single PA to one DAC/ADC pair, a quick port of DFE reference design (v2.1) from an existing Xilinx 16nm MPSoC device was accomplished, leveraging fabric commonality between the RFSoC and 16nm SoC for design reuse.

In this, Xilinx CFR IP was operating at 245.76 MSps (achieving 3% EVM at 7.5dB PAPR with TM3.1a signals) and DPD IP at 491.52 MSps (DAC/ADC operating in 2nd Nyquist using 3.93216 GSps clocks and 8x interpolation/decimation), with a composite signal 2c LTE20 + 1c LTE20 within instantaneous bandwidth of 160 MHz. The PA output is 45 dBm or 32 watts. After running DPD, the achieved ACP (shown on the right side of Figure 5) is 54.91 dBC and upper ACP is −55.14 dBC that complies with sufficient margin for the LTE spectrum emission mask requirements.

Figure 5 RFSoC setup for 2c LTE20 + 1c LTE with IBW of 160MHz

Xilinx All Programmable RFSoCs monolithically integrate high speed wide bandwidth RF-sampling data converters with fabric rich in-digital signal processing and compute resources to address diverse multiband requirements for 5G NR and LTE-Advanced Pro MIMO and massive MIMO radio system implementations. This technology addresses the challenges of massive MIMO by significantly reducing system footprint, power, and cost. The inherent programmability of the RFSoC devices and re-use of existing solutions enables faster time to market while allowing simple field updates to comply with emerging standards and newer algorithms and PA technology.

Paul Newson is a System Architect for wireless communication systems, Hemang Parekh is a Senior Engineering Manager, and Harpinder Matharu is the Director of the Communications Business, all at Xilinx.

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