Parasitic extraction must solve advanced node issues

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Integrated circuit (IC) designers move to advanced process technology nodes to leverage higher performance, density, and functionality, as well as reduced delay and power consumption, enabled by continuous dimensional scaling. Transitioning to new device architectures such as fin field-effect transistors (finFETs), fully depleted silicon on insulator (FDSOI), and gate-all-around (GAA) further extends gate length scaling, but leads to increased parasitic interactions between neighboring geometries [1]. New parasitic extraction (PEX) options for interconnect modeling ensure accurate capture of parasitic and layout-dependent effects for non-planar devices. In addition, these options can provide more efficient netlist input to downstream analysis. By adopting these advanced PEX solutions as part of their verification flows, designers can successfully realize the benefits of their advanced node designs.

Parasitic extraction challenges at advanced nodes

The introduction of finFETs, non-planar multi-gate structures, and nanowire metal-oxide semiconductor field effect transistors (MOSFETS) has added new complexity to the extraction process at advanced nodes.

FinFETs are a variation of traditional MOSFETs. They have a thin silicon fin inversion channel on top of the substrate, enabling the gate to have contact on both the right and left side of the fin (Figure 1). The use of finFETs allows manufacturers to scale down to smaller nodes; it currently appears that finFETs could sustain scaling until 2021 for high-performance logic applications [2]. The major method for improving finFET performance is to increase fin height while reducing the number of fins.
Figure 1 FinFETs provide significantly faster switching times and higher current density than traditional CMOS technology (Source: GLOBALFOUNDRIES; used by permission).

However, the International Roadmap for Devices and Systems (IRDS) states that beyond 2019, parasitics will be more dominant in the performance of critical paths. New GAA structures with vertical nanowires (Figure 2) will be necessary when there is no room left to scale the gate length down in finFETs [3].

Figure 2 GAA FETs provide lower power consumption and enhanced device performance, and are more compact than conventional planar transistors (Source: A. Hikavyy, et al.; used by permission).

The parasitic capacitance between gate and source/drain terminals of these new device types and the interconnect resistance increase with technology scaling. These effects negatively impact design performance. Designers are faced with the difficulty of reducing source/drain series resistance, as well as contact and interconnect resistance, to maximize the performance and power potential of this new technology.

It is possible to combat these detrimental parasitic effects to some degree with innovative design techniques. For example, TSMC uses a flying bit-line (FBL) and double wordline (DWL) approach to mitigate the RC wire load impact and improve SRAM array access performance for their 7 nm 256 MB SRAM [4].

However, given the criticality of parasitic delay, it is more effective and efficient to manage parasitics in 7 and 5 nm designs using a comprehensive approach that includes expanded interconnect modeling and extraction, as well as enhanced design analysis.

Interconnect modeling
Interconnect modeling can be split into three different sections:

- **Front-end-of-line (FEOL):** All of the IC fabrication layers that make up a device (transistors, capacitors, resistors, etc.).
- **Middle-of-line (MOL):** MOL layers connect a device to the metal wires and consist of a series of contacts and local interconnect.
- **Back-end-of-line (BEOL):** metallization layers where individual devices (transistors, capacitors, resistors, etc.) are interconnected with wiring on wafer.

Industry device models are used with simulation tools to model FEOL layers. For example, a common industry model used for finFETs is the BSIM common multi-gate (BSIM-CMG) model [5]. These device models mimic the way a transistor behaves with a compact model. The model captures how the drain current behaves vs. voltage, as well as capacitance vs. voltage. Although much work has been done to include layout-dependent effects in the device models [5], the compact models have limited methods to capture parasitic effects, so a PEX tool is often used to capture layout-dependent effects. The simulation tool uses the BSIM-CMG model to characterize behavior in the gate region, and uses parasitic resistance and capacitance extracted by a PEX tool to include the layout-dependent effects. To avoid double counting, design teams must agree on the division of the design layout between the device model and extraction rule deck, so that nothing that is already incorporated into the device model is also extracted by the PEX tool.

Due to the three-dimensional (3D) geometry of the finFETs used at advanced nodes, the coupling effects between devices and interconnect are more noticeable in finFETs [6]. Also, because the BSIM-CMG model uses an ideal single-fin model, there is a lack of layout-dependent effects. As a result, field solvers are required to accurately measure circuit performance in MOL layers because they capture 3D effects more precisely, making them obligatory for accuracy around the finFETs [7]. The PEX tool must also extract MOL layers accurately, and be well-integrated with the device model. MOL modeling also includes contact bias modeling, where bias refers to the extension of an edge. For advanced nodes, the diffusion tap has pitch-dependent bias behavior, which must be handled by the RC extractor. Finally, local interconnect modeling is also becoming increasingly important. M0/M1 local interconnects show increasing resistance with line width and process scaling, and M0 and contact emerge as prominent contributors to local interconnect resistance at the 5 nm process node [8].

BEOL consists of the metal layers and the vias that connect them. One significant challenge is the modeling of potential mask misalignment in litho-etch multi-patterning (MP), which is used extensively at 10 nm and below. At larger nodes, this misalignment is approximated by simply adjusting all coupling capacitance values either up (DPworst) or down (DPbest). At smaller nodes, not only is MP mandatory, but the designers perform the layout decomposition instead of the foundry. On the design side, that means that more accurate extraction modeling can be performed during verification.

One possible technique modifies the dielectric constants to obtain an equivalent coupling capacitance change representative of the mask misalignment [9]. If two geometries are on the same mask, there is no misalignment. If two geometries are on different masks, then the masks can shift relative to each other, and the change in coupling capacitance can be modeled (Figure 3). With mandatory coloring at these smaller nodes, it is possible for the extraction tool to more accurately compute coupling capacitance shifts due to mask misalignment.
Figure 3 Mask shifts in MP designs can lead to changes in coupling capacitance. PEX tools must be able to anticipate and account for these potential shifts.

Another method is to create custom corners that are offset-based [9]. Process corners are used when a certain metal layer has a nominal thickness, but in reality, the layer may be slightly thinner or thicker. The dielectric thicknesses can also vary. Foundries publish different rule decks that contain these variances, which lead to the capacitance values either increasing or decreasing, or the RC values increasing or decreasing. At advanced nodes, foundries are now publishing process corners that have either a higher or lower standard deviation. Designers can either use the tight process corners (where the standard deviation in thickness is smaller) so their designs can be more tightly tuned for performance, or they can use the regular process corners (with a larger standard deviation) to make their design more robust to larger swings in corners, at the sacrifice of either area and/or performance (Figure 4).

Figure 4 More accurate modeling of corners at advanced nodes lets designers optimize layouts to meet design goals.

Retargeting is a data preparation operation performed on a layout that modifies the drawn BEOL
interconnect layers to enhance yield and achieve performance targets (Figure 5). For example, systematic defects that occur in the manufacturing process, such as end-of-line via metallization overlap, can be minimized by increasing the line extension beyond the minimum value, reducing the risk of improperly formed vias. Retargeting is different from optical proximity correction (OPC) and resolution enhancement technology (RET), which are performed by the foundry or fab after tapeout.

![Figure 5](image)

**Figure 5** Retargeting a layout can improve both yield and performance.

Retargeting becomes more important and complicated in advanced nodes, because the dimension delta between the drawn and retargeted layout must preserve certain spacings. For example, the line-end, corner, and concave effects for short wires must all be handled appropriately. The amount by which a line-end can be extended has a limit. PEX tools must be able to perform retargeting while not encroaching into the forbidden area (Figure 6).

![Figure 6](image)

**Figure 6** PEX tools must recognize design limits when retargeting.

So, parasitic extraction tools must accurately address the new interconnect modeling requirements for any process layer to ensure that once the silicon is manufactured, it will work as intended.

Efficient corner processing

Multi-corner interconnect extraction is a requirement for both custom and digital designers. Not only voltage and temperature, but also cell characterization, block extraction, and signoff must be completed at multiple process corners. MP at advanced nodes adds even more corners. For example, at 7 nm, there are nine process corners, and each process corner also has one or more MP corners. These MP corners are included in the foundries’ process corner technology files. Because designs
are also growing in complexity at each successive node, a big challenge for 7 nm designers is evaluating the design at all mandatory or recommended corners without incurring additional cycle time during the signoff phase. It is imperative that parasitic extraction tools handle these complex modeling requirements with efficient processing.

In the past, each process corner meant a separate extraction run. For nine process corners, the designer had to execute nine different jobs, which required either adding machine resources or extending the extraction time budget [10]. To solve this challenge at advanced nodes, some PEX tools can perform simultaneous multi-corner extraction, in which all process, multi-patterning, and temperature corners are extracted in a single run (Figure 7). The user specifies the desired combination of corners to extract and netlist. For this flow, layout vs. schematic (LVS) checking is run once, followed by simultaneous multi-corner extraction that generates the corresponding parasitic netlists.

![Figure 7](image.png)

**Figure 7** Traditional individual corner processing vs. simultaneous multi-corner extraction.

**Electrically-aware reduction**

Parasitic extraction adds large amounts of parasitic capacitance, resistance, and inductance elements to the netlists for simulation with post-layout analysis tools. At advanced nodes, the number of elements results in netlists that can strain the capacity of downstream simulators. Designers must tailor extraction to maximize accuracy while minimizing the amount of parasitic data. There are several ways to reduce a parasitic netlist. Some methods eliminate elements based on threshold or tolerance. A more efficient reduction mechanism like time constant equilibration reduction (TICER) is electrically aware, producing a smaller RC network while controlling the error. TICER can be used for all design flows from analog, full custom to digital sign-off. [11]

For a 128K SRAM design, the timing simulation ran 30% faster on a parasitic netlist with TICER reduction when compared to an unreduced netlist (Figure 8), while the simulation error was within 2% compared to the unreduced netlist (Figure 9).
Electromigration and self-heating analysis

Due to the increased density and the use of finFETs in 7 nm technologies, self-heating and its effect on electromigration (EM) is becoming a big issue. EM is a process that happens naturally when computer chips run. It refers to the displacement of atoms in interconnect due to high current density. The electron flow pushes atoms out of their original location, which causes opens when there is a gap, or shorts when the protruding metal touches another metal interconnect. The current density $j$ shown in Figure 10 is the bottom factor, so increasing the current density reduces the mean time to failure.

$$MTTF = \frac{A}{j^n} \times e^{\frac{Q}{kT}}$$

Where:
- $MTTF$ is mean time to failure
- $A$ is a constant
- $j$ is the current density
- $n$ is a model parameter
- $Q$ is the activation energy
- $k$ is Boltzmann’s constant
- $T$ is the absolute temperature in K

Figure 10 EM analysis helps designers analyze reliability.
Because finFETs have low thermal conductivity due to a narrow conduction path, a lot of heat is transmitted upwards to the metal layers. With the increasing temperatures due to the finFETs’ lower thermal conductivity, it is important to take the temperature into consideration during EM analysis. Since EM current density levels decrease with an increase in temperature, designers must be able to measure how much heat is being transmitted by the transistors, and to lower the EM current density limit accordingly.

For a thorough EM/self-heating analysis of a design, the parasitic netlist generated by the PEX tool must contain several features needed by the EM tools: multiple device parameters (which are extracted during the LVS stage of the design flow and output in the parasitic netlist), layer mapping information, and device locations for each individual finger of the device. The netlist also contains parasitic devices and their layer, width, and location information. Having an accurate width value adjusted for OPC and chemical-mechanical polishing (CMP) improves the EM tool’s current density calculation accuracy. This netlist feeds into the EM analysis tool, which calculates how much current there is in all parts of the circuit. It can calculate both average current ($I_{avg}$) for power and ground nets, and root-mean-square current ($I_{rms}$) for signal nets. After EM analysis, the current density information is created and combined with the foundry-provided self-heating model to run a self-heating analysis. **Figure 11** shows an example of the design flow for analog, mixed-signal, and RF designs with the addition of EM and self-heating analysis.

**Figure 11** EM and self-heating analysis fit into existing design flows.

This analysis creates temperature maps that are then back-annotated to the EM tool to enable the increased current density violations with the new lowered threshold to be seen. For example, designers using a PEX tool like the Calibre xACT platform can view location information for both the finFETs and the parasitics:

*\[ I (MM0<1>:g MM0<1> g B 0.0 1.6250 0.4800) // $llx=2.4800 $lly=0.4800 \\
urx=2.4800 $ury=0.4800 $lvl=84 \]*
Based on the results of this analysis, the designer has various options to reduce current density. The main methods used are via doubling and wire spreading (Figure 12).

![Figure 12](image)

**Figure 12** Multiple design options help reduce EM susceptibility.

**Conclusion**

Advanced nodes require new and enhanced parasitic extraction processes that can resolve a variety of complex parasitic issues in these designs. New options for interconnect modeling ensure accurate capture of parasitic and layout-dependent effects for non-planar devices like finFETS, while simultaneous multi-corner extraction and accurate reduction handle complex modeling requirements with efficient processing. Providing device location information to the EM/self-heating analysis ensures current density violations can be accurately identified and mitigated. By introducing new and expanded parasitic extraction solutions such as these into their design flows, designers can successfully evaluate and mitigate parasitic issues in their advanced node designs, ensuring improved performance and reliability.

**Related articles:**

- Efficient parasitic extraction techniques for full-chip verification
- Parasitic extraction at advanced nodes
- Electromigration protection requires accurate interconnect modeling
- Parasitic extraction in the age of double-patterning
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References


