Improve accuracy of electrical system thermal simulation with full-circuit 3D modeling

Robin Bornoff - September 07, 2018

Typical 3D thermal simulation of electronics components assumes that all the power consumption the data sheets define is dissipated in the semiconductor. In the case of high current power modules, however, the power dissipation of the device's internal electrical distribution network can also become a significant factor. This tendency makes it essential to consider this heating effect in the simulation space, because considering only the semiconductors as the heat source may not be an accurate approach to use with current high-end and future applications.

The assumption that a device's power consumption is dissipated solely in the semiconductor can result in substantial errors in temperature-rise predictions when modeling electronic devices. Our studies, for instance, indicate that in commercially available components, power dissipation on the copper traces can be in the range of 30% of the total input power. These errors can be overcome by using an electro-thermal simulation approach that simulates the full electrical circuit, predicting the resistive heating in the power delivery network as well as the dissipation in the semiconductor. Solving for both the device's electric and thermal behaviour allows modelling of both power levels and distribution, thus improving the accuracy of temperature rise predictions.

Power dissipation distribution effects thermal simulation

The accuracy of a temperature (rise) prediction is predicated on the accuracy of the power dissipation, in terms of magnitude and distribution. A common assumption is that power is only dissipated in the active layer of the semiconductor chip. But for high current power electronic applications, an appreciable amount of power is dissipated in the rest of the power delivery system. As the trend of decreasing Rds(on) continues, the relative electrical resistivity, thus power dissipation, of the power delivery system will become increasingly significant. But, how can this trend be accommodated by simulation?

Take, for example, an IGBT (insulated-gate bipolar transistor) -- a three-terminal power semiconductor device primarily used as an electronic switch that combines high efficiency and fast switching. Circuits with IGBTs can be developed and modeled with various circuit simulating computer programs such as SPICE, Saber, and other programs. To simulate an IGBT circuit, the device (and other devices in the circuit) must have a model that predicts or simulates the devices’ response to various voltages and currents on their electrical terminals. For more precise simulations, the effect of temperature on various parts of the IGBT may be included with the simulation.

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Power, and potentially the temperature dependence of the power, can be predicted by solving for both the electric and thermal behaviour of a system. This is usually done using one of two standard approaches. The relaxation method couples two independent electro and thermal solvers together, passing temperature and power between them. The direct method solves for both electro and thermal behaviours in a single solver. Electro-thermal SPICE-type network solvers that use the direct method are becoming common.

**Taking real measurements of an IGBT**

We conducted a study to investigate how well the direct method works in the context of a full 3D electro-thermal simulation. The aim of the study was to verify the simulation model's accuracy in predicting the power dissipation distribution and the resulting variations in temperature increase.

We first ran an Infineon FS800R07A2E3 IGBT power-inverter module in the lab through a Mentor T3Ster system, which can be used to get accurate measurements of what is happening inside the chip. The IGBT module contains three half-bridge stages, and we selected the third phase’s low-side IGBT for testing. We distributed the power in the IGBT between two identical chips for better power management, and we tested the component in saturation mode. Specifically, we applied voltage through a 15-V gate to open up the device and switched between 500 A heating and 500 mA sensor currents to initiate a good power step on the semiconductor component.

The sample device (Figure 1) has powering terminals for the high current (3 and N3) with separate sensor terminals (C6 and E6) individually connected to the IGBT's emitter and collector. These separate sensor terminals allowed us to create a “true” Kelvin-probe setup, where the powering and the measurement lines were separated for the more accurate voltage drop measurement over the chip.
We assumed that the voltage drop on the metallization could significantly affect the results of the thermal transient tests. So, to check this we tested the sample's thermal resistance by powering and sensing on the main power pins (3-N3), and then powering on pins 3-N3 while sensing on the dedicated sensor pins, C6-E6. Because the system's temperature sensitivity primarily depends on the tested semiconductor, in both cases the measured temperature responses were the same. However, if we considered the internal metallization in our measurement, we got approximately 900 W heating power, but only 700 W if we directly measured on the semiconductor.

The measurement pins' location also heavily influences the calculated structure functions, or the measured thermal resistances. To verify the effect, we created an accurate 3D electro-thermal model of the setup and analyzed it.

**Tuning and calibrating the model**

An accurate, steady-state, 3D electro-thermal model requires well-defined electrical and thermal resistance properties, which means that the geometry, electrical resistivity, and thermal conductivity values must be determined and precisely described. To achieve this, we tuned the 3D electro-thermal model against a combination of the measured chip temperature, the chip’s transient
temperature response to a unit power step (Zth curve), and point voltage drops. We applied a 500-A boundary condition at Pin N3, 0V at Pin 3, and used Pin E6 and C6 to monitor the voltage drop over the IGBT chips.

**Figure 2** shows the stack-up section through one of the active IGBTs. The model provided a sufficiently detailed representation, including the chip mettallization, active layer, chip, solder, and DCB substrate. We designated all non-active IGBT and diode active layers, as well as the ceramic layer, as dielectric, isolating the electrical circuit to the power delivery network, metttallization layers, bond wires, and the two active IGBTs' chip and active layers.

The IGBT module has an integrated pin-fin heat sink at the bottom of the baseplate, cooled by a water jacket. We didn’t explicitly model the pin-fins and water jacket, however. Instead, we defined a contact thermal resistance between the bottom of the baseplate and a fixed temperature boundary condition over the area of the baseplate where the fins are. The electrical resistivity material properties of all the metallic objects were well-characterized, including temperature-dependent coefficients.

The two main unknowns were the active layer’s electrical resistivity and that of the doped silicone-based chip. The former was the most temperature-sensitive parameter and formed the basis of the calibration we performed. The latter had a value much smaller than that of the active layer, and was dependent on dopant concentration, so that value was less sensitive. We assumed a value of 2e-5 Ohm-m.

When analyzing thermal conductivity material properties, we found the two values most sensitive to the predicted temperature rises were the ceramic's thermal conductivity and the contact resistance
representing the non-modeled pin fins. So, our calibration procedure involved varying three parameters: the active layer electrical resistivity, the ceramic's thermal conductivity and thickness, and the contact resistance at the fixed temperature boundary condition. We varied these parameters until the 3D model in FloTHERM replicated our T3Ster measurements for the two measured voltage drops (N3-0 and E6-C6), the average steady-state chip temperatures, and $Z_{th}$ and the cumulative structure functions.

For our final calibration, we set the ceramic layer at 740 microns thick with a thermal conductivity of 105 W/mK, set the active IGBT layer's effective electrical resistivity at 0.115 Ohm-m, and set the contact resistance representing the pins and water jacket at 3.5e-5 Km$^2$/W. Although geometric measurements of all accessible geometry was possible, we made no destructive, sectioning measurements. As a result, the active layer's effective resistivity and thermal conductivity and the ceramic thickness might not be exact. However, the resulting effective electrical and thermal resistances were calibrated (Table 1).

<table>
<thead>
<tr>
<th>Measurement</th>
<th>N3-3 (V)</th>
<th>E6-C6 (V)</th>
<th>dTj (DegC)</th>
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</thead>
<tbody>
<tr>
<td>Measurement</td>
<td>1.812</td>
<td>1.4</td>
<td>75.8</td>
</tr>
<tr>
<td>Simulation</td>
<td>1.817</td>
<td>1.337</td>
<td>75.4</td>
</tr>
<tr>
<td>Error</td>
<td>-0.3%</td>
<td>4.5%</td>
<td>0.5%</td>
</tr>
</tbody>
</table>

Table 1 Voltage drop and chip temperature rise above ambient calibration results.

We used the same approach to simulate the transient temperature response to an increase in power of the system ($Z_{th}$) when performing the T3Ster measurement. Starting from a driving-current, steady-state, electro-thermal solution at $t = 0$ s, we conducted a transient thermal-only simulation and recorded the resulting chip average temperature vs. time curve (Figure 3). Although, in reality, T3Ster switches down to a sensing current and not zero at the start of the transient measurement, such currents are low enough that an assumption of no self-heating was valid.
Although the calibration against a measured transient thermal response does, in theory, calibrate the model for transient thermal behaviour, our intention was to further confirm the thermal material properties outside of the IGBT. This further confirmation was made to ensure that the predicted steady-state temperature rise was correct for the right reasons, not a consequence summing erroneous thermal resistances in the stack leading to a coincidentally correct overall thermal resistance (Rth). This confirmation approach helped us to ensure correct temperature prediction through the stack, not just the semiconductor’s temperatures.
What we learned about power dissipation

Under low current conditions (such as sensing), the IGBT's electrical resistivity was far greater than that of the rest of the circuit. The vast majority of the dissipated power occurred at the chip. At high currents, however, the relative resistivity of the chip decreased with respect to the rest of the circuit, and the assumption that all the consumed power is dissipated at the chip, becomes incorrect. The simulated power budget at the driving current of 500 A is shown in Figure 4.

![Figure 4 Simulated dissipated power budget for the IGBT module](image)

Out of the 912 W total consumed power, 64% was dissipated on the active layers of the two IGBTs, 4.7% in the bond wires, 1.4% in the metallization layers, and the remaining 29.6% in the rest of the power delivery circuit. The ratio of the voltage measurements at the four pins, N3-0 covering the entire circuit, E6-P6 covering the IGBT chips and bond wires, 1.4/1.812 V = 77%, provided us with a first-order indication of the power budget split between the active devices and the power delivery circuit.

Effects on power distribution in the active layer

For the current flowing up through the active layer, the metallization layer's effectiveness in spreading the current to the attached bond wires, as well as the proximity of the bond wires to the return part of the power delivery circuit, determined the distribution of current and thus the distribution of power within the active layer. The differences in the currents being carried by each bond wire are shown in Figure 5.
Bond wires nearer the 0-V return pin (top left) carried approximately 20% more current than those furthest from the return (top right). We assumed this occurred because of the reduced electrical resistance between the bond wires closer to the 0-V return compared to those further away.

This knowledge of actual electrical behaviour helps contribute to a more accurate prediction of heating. A thermal-only simulation would consist of an estimate of the power dissipation and its location. While the total power dissipation was readily measurable (full-circuit voltage drop measurement in conjunction with knowledge of the driving current), assuming that all the consumed power was dissipated in the active layer and that that dissipation was uniformly distributed would result in considerable temperature prediction errors. As shown in Figure 6, these assumptions result in the maximum temperature rise predicted at 34% higher, the location of the maximum temperature at a different point, and the temperature variation across the active layer as 30% greater than the electro-thermal simulation predicts.
Overcoming model limitations

Calibrating to a single driving current inside a device such as an IGBT is limited when using simulation only. FloTHERM assumes a single electrical resistivity material property, whereas the IGBT exhibits a non-linear IV relationship. This limits the general application of the calibration method to materials that exhibit a linear, through origin, IV characteristic. Our calibration methodology worked within this limitation by determining the (electrical) operating point by adjusting the active layer resistivity contribution so as to intersect the IV curve with the driving current line (Figure 7).
Calibrating the active layer’s effective electrical resistivity at the same driving current but at differing junction temperatures (via control of the ambient water jacket temperature), would enable determination of the temperature dependent coefficient of that electrical resistivity. This determination also might refine the accuracy of predicting power dissipation of the active layer, taking into account local variations in chip temperature and electrical resistivity. Defining a more generalized electrical material property by using an I vs. V vs. T characterized surface would allow for the full range of operating currents to be handled in simulation, including temperature dependency.

Another model limitation to consider is its dynamic response. When the IGBT module is in operation, the total power dissipation is comprised of a contribution from the DC losses and the losses that occur during switching. From a 3D transient modeling perspective, it is not tractable to consider resolving electrical switching timescales concurrently with the thermal timescales of the rest of the system.

An alternative approach would be to use a circuit simulator such as ELDO to perform a full transient electrical stimulation. Subtracting the DC contribution from the predicted instantaneous power
profile leaves the switching loss profile. That profile could then be time-averaged to derive the cumulative switching loss power. This cumulative value could then be modeled as a steady-state power source, collocated with the active layer objects in the 3D electro-thermal model, thus allowing the time-averaged switching losses to be considered in addition to the electro-thermally predicted DC losses.

It is clear, then, that legacy thermal simulation approaches assuming all consumed power is dissipated in the semiconductor can lead to 34% errors in temperature rise prediction for such power electronics applications. These errors result in the simulation being all but useless from a design perspective. Solving the full electrical circuit on a T3Ster calibrated FloTHERM simulation model, though, enables the distribution of power to be predicted, which leads to highly accurate temperature rise prediction that can then be used to judge the thermal compliance of a proposed design under operating conditions. This evaluation itself is not possible without a combined “test and simulation” methodology.

Robin Bornoff is the market development manager for the Mechanical Analysis Division of Mentor, a Siemens business. Having joined in 1996 as a support and applications engineer, he is now responsible for the identification of emerging technologies and workflows for inclusion in the Mechanical Analysis Division products roadmaps. Robin received a bachelor's degree in Mechanical Engineering in 1992 and a PhD for CFD research in 1996 from Brunel University.

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