Direct-RF DACs for high-speed communications

Bonnie Baker - December 19, 2018

Consumers have an unquenchable demand for higher video, data, and voice bandwidths through the cable, satellite, and terrestrial conduits. For the next evolutionary step, consumers will want more bandwidth at a lower cost. To meet this challenge, OEM designers will need to offer communications equipment that supports higher capacity at a lower solution cost.

Modern wireless radio transmitter designs encompass real IF (intermediate frequency) transmitters, complex IF transmitters, and zero-IF transmitters. At present, these transmitters continue to shuffle data through analog paths. There are limitations in the analog domain which impact the performance, capacity, and cost of the system, however.

To meet the demands for higher bandwidth communications, IC manufacturers have developed direct-to-RF architectures that provide excellent spurious, low-noise performance with output update rates in the giga-samples-per-second (Gsps) range.

In this article, we will compare the direct-RF transmitter to the analog-RF structure. We will examine the evolution of the direct-RF, digital-to-analog converter (DAC) transmitter and see how it simplifies RF design and achieves higher capacity at a lower solution cost.

**Analog complex IF transmitter**

Traditional transmitter architectures use the superheterodyne principle, where a local oscillator (LO) and a mixer generate IF. **Figure 1** provides a basic diagram of an analog complex-IF transmitter.

**Figure 1** Analog complex-IF to RF-transmitter multi-device solution

A complex baseband digital input signal commonly uses an LVDS (low-voltage differential-signaling)
interface across two channels: an in-phase or “I” data channel, and a quadrature or “Q” data channel. Some systems use interpolation on the complex baseband I and Q signals by a factor R. Interpolation eases the requirements for the analog filter while also reducing in-band noise. The digital complex modulator and a numerically controlled oscillator (NCO) mix the signal in frequency (“heterodyning”). Dual DACs then convert the digital I and Q IF carriers into analog signals.

Now in the analog domain, the two parallel signals flow through lowpass filters to their respective I and Q mixers. These mixers are fed by an LO, which has a straight-through I path and a 90° phase-shifted Q path. Finally, the two signals are combined through a summation block, resulting in a complex modulated signal at the desired frequency.

The use of this conventional transmitter architecture produces an LO “image” artifact. Before the final voltage-gain amplifier (VGA) stage, a bandpass or SAW filter is used to reduce the magnitude of the unwanted image. The filter rolloff must be sharp and the LO frequency stable enough to reduce the unwanted sideband image (at fLO - fIF) without adversely affecting the desired signal (Figure 2a).

As Figure 2a shows, any analog mismatch (phase or gain error) between the I and Q paths results in a sideband image. In addition, the LO can feedthrough the mixing stage and appear in the RF output spectrum as LO leakage. These non-ideal artifacts limit the performance of an analog system, requiring additional filters and calibration circuitry, which in turn increases design complexity and cost.

This architecture has a limited output signal bandwidth because the input sample rate of the dual baseband interpolating DACs are constrained by the amount of data transferred over the relatively slow LVDS or CMOS interfaces. Often this bandwidth limitation in turn requires different AQMs (analog quadrature modulators) or multiple sets of hardware, each with different LO frequencies, to support different RF bands.

**Evolving to an RF-DAC solution**

The baseband signal generated by the input is digitally upconverted using the I/Q interpolators, digital quadrature modulator (DQM), and NCO. The I/Q data paths in the DQM are perfectly matched (as a result of the digital implementation), which prevents the development of a sideband image (Figure 2b). The absence of the sideband image and LO carrier frequency eliminates the need for costly and complex SAW filters. The system then presents the signal to the RF DAC core, which produces the RF output.
At the JESD204B input of the RF-DAC transmitter shown in Figure 3, the interpolators (↑R) increase the DAC sample rate relative to the input data sample rate.

**Figure 3** JESD204B input to RF-DAC transmitter enables higher input data sample rates. JESD204B is a high-speed serial interface that allows Gbps data rates.

The RF-DAC transmitter replaces the analog LO with a digital NCO, eliminating the LO feedthrough or leakage to the analog RF output. The output bandwidth of the RF DAC and the Nyquist bandwidth (fDAC/2) determine the maximum RF frequency.

The input structure of the RF-DAC transmitter accommodates high-speed 5G signals across the JESD204B serial interface, creating a system that has higher signal bandwidths than the analog complex-IF RF-transmitter.

Compared to the analog complex-IF implementation, the RFDAC transmitter architecture simplifies and reduces the cost of this application, while increasing the bandwidth performance and reducing the PCB footprint.

**Architecture comparison**
The RF-DAC offers three opportunities to reduce the overall cost of the system, which includes PCB space, component count, and simplified design (Table 1).
The wave of the future in RF transmitters is before us. Although popular analog transmitter topologies are effective at lower frequencies with higher noise and cost, the speed of wireless data transmission is becoming beyond their capability. The next evolutionary step is the direct-to-RF transmitter. These interpolating and modulating 16-bit RF DACs provide improved spurious low-noise performance and simplified design. Their input data rates in the Gsps region provides the high bandwidth requirements needed for 5G technology at a lower cost.

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