High-voltage current sensing with low-voltage transistors

Seagan Yi-O'Kelly - May 14, 2019

Current monitoring has become simpler because of the availability of dedicated integrated circuits. Current monitoring integrated circuits are readily available and under most circumstances do an excellent job, as do various instrumentation amplifiers, so building a current monitor using discrete devices may seem redundant, however there are circumstances where a circuit using discrete components might be the best approach especially if readily available low voltage parts can be used.

The circuit in this Design Idea resulted from the need to monitor current in both rails of a servo system’s +180/−180V power supply. Figure 1 shows the relevant part of the circuit for monitoring the negative rail. The circuit monitoring the positive rail replaces npn with pnp devices. Best results are obtained using inexpensive dual transistors and 1% resistors for setting Iref and for Re1 and Re2. Rsense should be 0.1% and adequately rated for power dissipation.
Inspiration for this circuit and all those that use this topology derives from the current mirror topology and the notion that a varying current in Rsense, and therefore the voltage across Rsense, varies the current in Re2, and therefore the voltage across Rc1, in a linear fashion.

The circuit of Figure 1 owes its utility to Re1 and Re2. Making Iref fairly small and Re2 and Re1 very large and equal in value increases the voltage at the emitters relative to the voltage across Rsense. This in turn decreases the change in the output device’s Vce when the load is varied between no load and full load.

It is therefore possible by judicious selection of Iref, Re1, Re2, Rc2, and Rc1 to prevent Q2 being driven into saturation and also to not exceed the transistors maximum operating voltage. Bear in mind that hoe=I(collector)/V_A (Early Voltage) implies that reducing the change in Ic also reduces the variation in β which in turn improves linearity. Rc is the sum of Rc1 and Rc2 so the ratio Rc1/Rc determines the offset at Vout−, under no load. The voltage generated across Rsense at full load determines the change in current in Re2 and Rc1 and therefore the full scale output at Vout−. Once a value for Iref is established, it is a simple matter to calculate the desired no load voltage across Rc and Rd. The effect of a varying Vce on Q2’s β is significantly reduced by the use of emitter resistors and inspection of the simulation data shows that the change in β has relatively little effect on the correlation between load current and output voltage. Using a configuration similar to a Wilson current mirror is probably unnecessary in view of the results achieved.
Figures 2 and 3 show alternative solutions for the constant current source to generate Iref. If Vss is stable and ripple free the constant current generator can be omitted, and a value of Rd can be selected to provide Iref.

![Image 1](image1.png)

Figure 2 An alternative solution for the constant current source to generate Iref.

![Image 2](image2.png)

Figure 3 FET bias is setup so that on startup Iref will not cause Vce or Vds to exceed the maximum value.

Figure 4 inverts Vout−, removes the offset, scales the output to the desired range, and can filter the output to deal with supply ripple or load spikes. The circuit can be simplified to just invert Vout− if a microcontroller with an ADC is used.
Figure 4 Inverting Vout− removes the offset, scales the output to the desired range, and can filter the output to deal with supply ripple or load spikes.

If $V_{Re1}$ is at least 10 times greater than $V_{Rsense}$ at full load, then the Q2 will not saturate and

$$V_{Rsense} = (I_{load} + I_{ref}) \times Rsense$$  \hspace{1cm} 1$$

$$V_{Re1} = 10(V_{Rsense(full \ load)})$$  \hspace{1cm} 2$$

$I_{ref} = I_{Re1}$, and at no load i.e. $I_{load} = 0$ therefore:

$$Re1 = V_{Re1} / I_{ref} = Re2$$  \hspace{1cm} 3$$

$V_{ccs}$ is the voltage across the constant current source and $I_{Re1} = I_{ref}$ to a close approximation, and $V_{be}$ can be taken as 0.6 to 0.65V:

$$Rd = (V_{ss} - (V_{ccs} + V_{be(Q1)} + V_{Re1})) / I_{ref}$$  \hspace{1cm} 4$$

$V_{ce}$ is the desired maximum voltage across Q2, and at no load. $I_{Re2}$ is approximately equal to $I_{ref}$, therefore:

$$Rc = (V_{ss} - V_{ce}) / I_{(Re2)} \approx (V_{ss} - V_{ce}) / I_{ref}$$  \hspace{1cm} 5$$

The desired offset voltage at Vout− at no load determines the value of $Rc1$:

$$Rc1 \approx (Rc \times V_{out−(offset)}) / V_{Rc}$$  \hspace{1cm} 6$$

An estimate of $I_{Re2}$ at full load can be made because $I_{(Rsense)} = I_{ref} / 10$:

$$I_{Re2(full \ load)} \approx 1.1 \times I_{ref}$$  \hspace{1cm} 7$$
At maximum load current the full-scale value of $V_{out^-}$ is approximately:

$$V_{out^-\text{(fullscale)}} - V_{out^-\text{(offset)}} \approx Rc1 \times I_{\text{R sense(full load)}}$$

LTspice was used to produce the following curves to show the circuit’s linearity, the effects of filtering, and $V_{ce}$ and $V_{ds}$ during circuit operation. The load current ramps from 0 to 1 amp and the output voltage is overlaid on the load current. The results are similar to the actual circuit performance. Filtering prevented trips due to short duration spikes in the load current. Isolation may not be necessary but should always be considered when designing high-voltage circuits.

Figure 5 Vout without 25nF cap at C1 in Figure 4

Figure 6 Vout with 25nF cap at C1 in Figure 4

Figure 7 Voltages on the active devices

For some background on current mirrors and the Widlar and Wilson current source, see:

- **Electronic Circuit Design**, Ch 7.3, Savant, Roden, Carpenter
- **Microelectronic Circuits and Devices**, Ch 8.3, Horenstein
- **Principles of Electronics**, Part 1 Ch 5.3 & Part 2 Ch 11.5, Ian B Thomas

Seagan Yi-O’Kelly has a background in plant automation and analog design.
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