Current feedback (CFB) amplifiers can exhibit high gain peaking and become unstable, and for various reasons even turn into oscillators. The two major causes for amplifier instability are making the value of the feedback resistor too low, and introducing parasitic input and output capacitances with regard to ground. While small capacitances cause the amplifier’s frequency response to peak at high frequencies, high capacitance values can force the device into self-sustaining oscillations, where it ignores any input signal stimuli.

This article provides design tips on how to ensure amplifier stability. Following the dos and don’ts enables the reader to design stable amplifier circuits without delving into the mathematics of the underlying principles.

There are three main ways to minimize the effects of parasitic capacitances on the amplifier’s stability:

1. Good layout techniques to minimize parasitic board and probe capacitances
2. Use the CFB amplifier manufacturer’s specified feedback and gain resistor values, as these provide sufficient phase margin to tolerate small parasitic capacitances
3. Use compensation techniques that minimize peaking of the frequency response and overshoots in the pulse response

Board layout tips

Achieving optimum performance with CFB amplifiers requires careful attention to board layout parasitics as well as external component types and resistor values. Referring to Figures 1 and 2, the following recommendations help optimize circuit performance:

- Buffer the power supply pins with decoupling capacitors for low and high frequencies. For high frequencies use 100nF and 100pF capacitors in parallel and place them less than ¼ inch (6mm) from the supply pin. For low frequencies, use 6.8µF tantalum capacitors, which can be placed farther away from the amplifier, and allows them to be shared among other devices. Avoid narrow power and ground traces to minimize trace inductance, particularly between the power supply pins and the decoupling capacitors.
- Because the amplifier’s output and inverting input pins are the most sensitive to parasitic capacitance, connect the output resistor, RS (if required) close to the output pin, and the feedback and gain resistor (RF and RG) close to the inverting input. These resistors isolate their respective pins from any trace capacitance.
- Design placeholders for RIN and CIN at the non-inverting input. These might be required to compensate the gain peak caused by the parasitic capacitance (CPI) at the inverting input.
Determine whether an output isolation resistor is needed. Low parasitic capacitive loads (< 5pF) often do not need an RS. Also, higher parasitic output capacitances can be driven without RS, but will require a higher closed-loop gain setting.

Maintain ground and power plane-free areas around the input and output pins to minimize the build-up of AC-ground related capacitances. Elsewhere on the board, the ground- and power-planes should remain unbroken.

Connect each test point through a 100Ω resistor to the trace to be measured. This resistor isolates the probe capacitance oscilloscope from the signal trace.

Figure 1 CFB amplifier with parasitic capacitances and compensation components, $R_S$, $R_{IN}$, and $C_{IN}$. 
Manufacturers of CFB amplifiers commonly specify multiple $R_f$ values, each corresponding to a different gain setting. Applying the recommended resistor values ensures optimum performance without (or only little) gain peaking or bandwidth reduction. Deviating from these values modifies amplifier performance. Figure 3 depicts this by using different $R_f$ values for a signal gain of two. The optimized and specified value of $R_f = 1.1k\Omega$ for this gain shows optimal performance. However, when raising $R_f$ to 1.5k$\Omega$, a reduction in bandwidth occurs, and when lowering $R_f$ to 600$\Omega$, gain peaking occurs (Figure 4).

Therefore, to achieve optimum performance, follow the manufacturer’s recommended $R_f$ values.
Figure 3 Using $R_F$ values specified in the data sheet ensures best performance.

Figure 4 Deviating from the specified $R_F$ values causes gain peaking or reduced bandwidth.

**Compensating the effects of parasitic capacitance**

To distinguish between the parasitic capacitance at the input ($C_{pi}$) and the output ($C_{po}$), the pulse-response test can be applied. $C_{pi}$, which is usually smaller than $C_{po}$, causes short signal overshoots,
while $C_{po}$ often results in prolonged signal ringing (Figure 5). Of course, the situation is reversed if $C_{pi} > C_{po}$. This however, is rarely the case.

![Image of Figure 5](image-url)

**Figure 5** Signal overshoots due to $C_{pi}$ versus signal ringing due to $C_{po}$

**Parasitic input capacitance**

**Parasitic input capacitance, $C_{pi}$**

The parasitic capacitance at the inverting input ($C_{pi}$) is usually small (0.5 to 5pF) and consists of layout stray capacitance and the inherent shunt capacitance of the surface mount resistor, $R_{v}$. Together with $R_{v}$ and $R_{g}$, $C_{pi}$ forms a low-pass characteristic in the amplifier feedback path, which translates into a high-pass characteristic in the amplifier transfer function $V_o/V_i$.

This high-pass characteristic can be compensated with an R-C low-pass filter at the non-inverting amplifier input. For this purpose, the input capacitance at the noninverting input must match the parasitic capacitance at the inverting input ($C_{in} = C_{pi}$), and $R_{in}$ must be made equal to the parallel combination of the feedback and gain resistors ($R_{in} = R_{v}||R_{g}$).
Figure 6 and Figure 7 show the frequency and pulse responses for the circuit in Figure 1, when the amplifier operates at $G = 2$, where $R_F = R_G$ are the manufacturer specified resistor values for best performance. Other observations made in Figure 6 and Figure 7 include:

- For CPI = 0, the frequency and pulse responses in black show neither gain peaking nor overshoots. The nominal gain is 6dB and the pulse amplitude is ±200mV for ±100mV test input at 10MHz.
- For CPI = 5pF, however, the frequency and pulse responses in red show gain peaking of close to 21dB and overshoots of ±1V.
- For the compensated case (blue curves), where $C_{IN} = CPI = 5pF$ and $R_{IN} = RF||RG = RF/2$, the
frequency and pulse responses show a reduction in gain peaking and overshoot down to 0.5dB and ±45mV respectively.

**Parasitic output capacitance, \( C_{po} \)**

The parasitic capacitance at the amplifier output (\( C_{po} \)) also includes layout stray capacitance, but the lion share usually comes from larger load capacitances, such as junction capacitances of transient suppressors and current steering diodes, cable capacitances, and input capacitances of analog-t-digital converters or other amplifiers. The total value of \( C_{po} \) can therefore vary from as little as 20pF up to several 100pF.

As mentioned before, small parasitic output capacitance often have little effect on the transfer function, while large \( C_{po} \) values can cause high gain peaking with prolonged ringing in the pulse response. **Figure 8 and Figure 9** depict the impact of a small 20pF output capacitance. The resulting gain peak is less than 1dB, showing only small overshoots of less than 30mV. If there is a need of compensating \( C_{po} \) at all, raising the \( R_F, R_G \) resistor values slightly will be sufficient.

![Figure 8](image-url) **Figure 8** Small \( C_{po} \) value compensated with higher \( R_F \) value
In strong contrast, the compensation of large output capacitance is necessary. For the uncompensated case, **Figure 10 and Figure 11** show some 15dB of gain peaking in the transfer function accompanied by prolonged ringing in the pulse response for a $C_{po}$ of 500pF (red curve). Raising the $R_e$, $R_c$ resistor values shows only little improvement (blue curve). However, implementing a series resistor ($R_s$) isolates the amplifier output from the capacitive load (see Figure 1 circuit). In this simulation, a small $R_s$ value of only 3.9Ω was needed to reduce the gain peak to less than 0.5dB, while reducing the signal overshoot from ±400mV down to ±50mV.
You can ensure amplifier stability by following the design tips highlighted in this article, and the summary tips highlighted here:

- Apply good layout techniques to minimize parasitic capacitance in the first place
- Buffer supply voltage rails for low and high frequencies using 6.8μF, 100nF, and 100pF capacitors
- Insert 100Ω resistors between a test point and the trace to be measured to isolate probe capacitance from signal trace
- Stick to the data sheet’s specified resistor values
- Perform initial pulse-response test to distinguish between parasitic input and output capacitance
- Compensate for parasitic input capacitance through an R-C low-pass at the non-inverting signal input
- Compensate for low parasitic output capacitance by raising the RF and RG values
- Compensate for large parasitic output capacitance by inserting a small isolation resistor, RS

For more amplifier information, visit this page.

**Figure 11** Compensation through R_s shows drastic improvement in pulse response

**Tom Kugelstadt** is a principal applications engineer with Renesas Electronics America where he defines new high-performance analog products for industrial systems.

**Related articles:**
- Unique compensation technique tames high-bandwidth voltage-feedback op amps
- In defense of the current-feedback amplifier
- Input and Output Voltage Range Issues for High Speed CFAs and FDAs, Insight #2
- Voltage- and current-feedback amps are almost the same
- High-voltage current-feedback amplifier is speedy
• High performance current feedback amplifiers at your service