Dual-voltage supply powers SIM card
Larry Suppan, Maxim Integrated Products, Sunnyvale, CA

Global-system-for-mobile-communication phones have a subscriber-identification module (SIM) that allows local wireless providers to recognize the user and his or her billing information. Although most SIMs are changing to 3V operation, they also accommodate 5V as well during the transition. IC1 in Figure 1 combines a step-up dc/dc converter with a linear regulator, allowing it to regulate up or down for a range of input voltages. It offers hardware-selectable fixed outputs of 3.3 and 5V; however, 3.3V is out of spec for a 3V SIM card. With properly chosen R1/R2/R3 values, you can switch the regulated output between 3 and 5V (or any other two outputs within the allowed range) by applying digital control to the power-good input (PGI). The power-good output (PGO), the output of an internal comparator, then changes the IC’s feedback by grounding the node between R2 and R3. If the power-good comparator is in use, you can implement the digital control using the 3/5 input and an external MOSFET (Figure 2).

You can obtain a regulated 3 or 5V output, according to digital control applied to the power-good input (PGI).

This circuit provides the same outputs as the circuit in Figure 1 without tying up the internal power-good comparator.
Design formulas simplify classic V/I converter

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Figure 1 shows a classic voltage-to-current (V/I) converter. You can select the resistor values such that the output current in the load, \( I_L \), varies only with the input voltage, \( V_{IN} \), and is independent of \( R_L \). The circuit is widely used in industrial instruments for supplying a 4- to 20-mA signal. The circuit has its limitations, however, because the resistor values must be quite accurate to obtain a true current source. The literature describing the circuit provides design methods that are for special cases or are for approximate designs. This Design Idea gives two simple design formulas you can use to determine the component values that produce a true current source. It also provides a general formula for the output current, \( I_L \), for any selection of resistor values, not just the constant-current selection.

For a true current output, \( I_L \), as a function of the input voltage, \( V_{IN} \), you must satisfy the following two equations:

\[
I_L = \left( \frac{V_{IN}}{R_1} + \frac{R_2}{R_X} \right)
\]

\[
R_3 = \left( R_2 + R_X \right) \frac{R_4}{R_1}
\]

In Equation 1, you can arbitrarily select any four of the terms and then determine the fifth term by solving the resulting equation. In Equation 2, you can arbitrarily select either \( R_1 \) or \( R_2 \) and then determine the unselected resistor after substituting the applicable terms from Equation 1. For example, you can solve Equation 1 for \( R_2 \) when \( I_L = 20 \text{ mA}, R_1 = 100 \text{ k}\Omega, R_2 = 0.1 \text{ k}\Omega, \) and \( V_{IN} = 4 \text{ V} \) yields \( R_X = 49.9 \text{ k}\Omega \). Now, let \( R_1 = 100 \text{ k}\Omega \) and, with Equation 2, solve for \( R_3 \) as follows: \( R_3 = \left( 49.9 \text{ k}\Omega + 0.1 \text{ k}\Omega \right) / 50 \text{ k}\Omega \). This example configures a design for the popular current source of 4 to 20 mA. In a second example, if \( R_X \) changes from 100 to 400\( \Omega \), the feedback changes fourfold, and you would expect that the output current would change fourfold, to 1 to 5 mA. You can check the result by substituting in the general formula for the output current:

\[
I_L = \frac{V_{IN}(KR_2 + R_X)}{R_1}
\]

\[
\left( R_1 + R_2 + R_X \left( \frac{R_1 + R_2}{R_2} \right) - R_1 \cdot \left( \frac{KR_2 + R_X}{R_2} \right) + R_X(R_1 + R_2) \right)
\]

\[
\text{where } K = 1 + \frac{R_3}{R_4}.
\]

When the complete coefficient (the terms inside the square brackets) of \( R_X \) equals zero, a true current source results, and equations 1 and 2 are valid. Note that substituting the values from the first example above forces the coefficient to zero. Substituting the values from the second example above results in the following expression:

\[
I_L = \frac{V_{IN} - 0.06R_L + 59.96}{0.06R_L + 59.96}.
\]

With \( R_1 = 0.2 \text{ k}\Omega \) and \( V_{IN} = 4 \text{ V}, I_L = 5.019 \text{ mA} \). Then, with \( V_{IN} = 0.8 \text{ V}, I_L = 1.003 \text{ mA} \). Thus, after changing the feedback resistor by 4-to-1, you still have currents close to the 1- to 5-mA standard.

Now, let \( I_L = 5.02 \text{ mA} \) when \( R_1 = 0 \Omega \); thus, the circuit is still almost a perfect current source. This result is unique, as you can convert from 4 to 20 ma to 1 to 5 mA by changing only one resistor. You can configure the less used standard of 10 to 50 mA by making \( R_X = 100/2.5 = 40 \Omega \).

To vote for this Design, Circle No. 316

Rail-to-rail op amp provides biasing in RF amp

Frank Cox, Linear Technology Corp, Milpitas, CA

It is often useful to monitor the dc level of an RF signal. However, most RF systems use capacitive coupling; thus, the dc information is lost. The circuit in Figure 1 is an RF amplifier comprising two monolithic microwave integrated circuits (MMICs), IC1 and IC2, and a quad rail-to-rail op amp (IC3, an LT1633). IC3A restores the dc level at the output. Inductors at both the input and the output of the op amp isolate the amplifier from the RF signal. The isolation is good practice, because frequencies higher than the bandwidth of the op amp can undergo rectification in the amplifier’s input stages, thereby introducing offset. MMICs IC1 and IC2 are Hewlett-Packard HP MSA-0785 devices, which have an inverting gain of 13 dB; the result is a total gain of approximately 26 dB and a noninverted signal. IC1 and IC2 have a 3-dB bandwidth of approximately 2 GHz. The 1.5-nF blocking capacitors set the low-frequency cutoff at 2 MHz.

IC1 and IC2 have a 1-dB compression point of 4 dBm, or 1 V p-p, into 50\( \Omega \), allowing for an input level as high as 18 mV.
rms. The maximum output current of IC3A, typically 40 mA with a single 5V supply, limits the dc level on the output to 2V into 50Ω. The output saturation (low) voltage of the LT1633, typically 40 mV, sets the minimum pedestal voltage. IC4 and IC5 use constant-current bias sources to stabilize their gain with respect to temperature.

Two other sections of the quad op amp, IC3B and IC3C, form active 22-mA current sources. You can make the voltage dividers on the noninverting inputs of IC3B and IC3C adjustable to trim the gain of the RF amplifier. The rail-to-rail inputs of IC3 allow the circuit to operate to within 110 mV of the positive rail. (DI #2467)

**Figure 1**

A simple op-amp-follower circuit with the aid of inductive blocking restores the dc level of an RF signal.

---

**Circuit multiplexes automotive sensors**

*Adil Ansari, Delphi-Delco Electronics, Kokomo, IN*

Often, a μC limits the number of input-capture lines to accommodate the various types of automotive sensors with pulsed outputs, such as vehicle- and engine-speed sensors. The circuit in Figure 1 uses discrete components to multiplex two sensors with open-collector outputs into a single output, thereby sharing one input-capture line of the μC. The μC selects the sensor whose output you will measure. You can apply this approach to sensors whose outputs are

**Figure 1**

You can multiplex the output signals from two sensors into one input-capture line in a μC.
amenable to time-sharing and do not require continuous monitoring, such as position sensors. In Figure 1, Sensor 1 and Sensor 2 are outputs from two sensors using npn transistors with open-collector outputs. To enable Sensor 1 or Sensor 2, Q1a or Q1b, respectively, must turn on. A logic-low signal from the µC on the Select input turns off Q2 and Q1c. When Sensor 1 input goes low, D1 forward-biases, and Q1a turns on, providing a high signal on MUXED_OUT. When Sensor 1 input turns off (high-impedance state), Q1a turns off, providing a low signal on MUXED_OUT. Therefore, when the Select input is low, MUXED_OUT produces pulses that are inverted but synchronized with the Sensor 1 pulses. At the same time, Q1c and Q1b are on, turning off Q1a and disabling the Sensor 2 input.

Similarly, when Select goes high, Q2 and Q1c turn on, turning off Q1b and disabling the Sensor 1 input. At the same time, Q3 and Q1d turn off, allowing the Sensor 2 signal to turn Q1b on and off when Sensor 2 switches on (low) and off (high-impedance state), respectively. Therefore, MUXED_OUT produces pulses synchronized with the Sensor 2 input. You can change the values of R1, R4, R5, and R6 to meet the sensors’ requirements. D3 clamps MUXED_OUT to CMOS/TTL levels. The use of the MPQ3906, containing four pnp transistors in one package, minimizes the number of components. Similarly, you can obtain arrays of 1-kΩ resistors in a single package. (DI #2469)

Many low-current devices that require 65V supplies can operate reliably in a single 5V power-supply environment if you use an appropriate localized dc/dc converter to generate the −5V bias. Often, the capabilities and advantages of these 5V ICs far outweigh the minor inconvenience and added costs of an additional −5V-converter function. Many companies manufacture dc/dc-converter ICs and modules in a variety of power ratings and footprints. However, these typical dc/dc converters can be overkill for simple, single-chip applications that require only a negative bias voltage with low operating currents. For these applications, typical negative-voltage requirements range from −4 to −6V with a supply current of 1 mA, and requirements for the −5V supply are generally noncritical.

A lower cost alternative to conventional dc/dc converter modules for generating negative dc voltages from a positive supply is shown in Figure 1. Using an analog switch with two external capacitors and an external clock is a viable way to produce −25V from a 5V input for low-power, −5V needs. One approach uses only one phase of the clock (a); a second approach requires both phases (b).

![Figure 1](image-url)
tive supply uses a low-cost quad-swing switching inverter, which is used for generating an output voltage whose polarity is opposite that of the input voltage. Two charge-storage capacitors are also necessary, as with conventional converters. Unlike the conventional self-contained dc/dc converter approach, this circuit requires a single external clock input to sequence the switches on and off and approximately the same amount of board space. You can tap this clock from any 5V logic-gate output with continuous logic switches.

Charge-pump converters operate by first charging up one capacitor and alternately transferring that charge to another capacitor using a switching circuit. The switching circuit in Figure 1 alternately charges and discharges C1 and C2 to generate a −5V output from a 5V input. Integrated level translators and logic gates inside the ALD4213 analog switch provide the logic translation to convert a single 5V input to a ±5V logic swing.

The circuit closes two switches, S1 and S2, under clock control. During the first half of a clock cycle, C1 charges up to a voltage equal to the input voltage, V+. The next half-cycle of the clock control opens S1 and S2 and closes S3 and S4, C2 now connects across C1 through S1 and S3, and the charge on C1 subsequently transfers to C2 until the voltage across both C1 and C2 is equal. Notice the “inverted” polarity across C2, which forces the output voltage on C2 to be V−, or the opposite of V+.

Each subsequent clock cycle, which again begins with the closing of S1 and S2, causes C1 to charge up from the previous voltage to V+. After many repeated clock cycles, the voltage on C2 remains charged to a value equal to the negative of V+, or close to it; it performs the function of a voltage inverter, which is more commonly called a converter.

An alternative analog-switch-based converter uses the industry-standard 74HC4316 quad analog switch with level translator (Figure 1b). The circuit is similar to the circuit in Figure 1 but has different pin connections. This circuit also requires both phases of the clock. You can use an additional inverting logic gate to generate both clock phases if necessary. The recommended input is a logic clock that has a useful frequency range of 5 to 500 kHz.

Figure 1a’s single-phase design costs less than $1 in large quantities. The cost of the circuit in Figure 1b can be less than half the cost of the circuit in Figure 1a provided that both clock phases exist and that you don’t have to add an external logic-gate inverter. You can also integrate analog-switching inverters with other analog functions in a custom ASIC; the ALD4213 and ALD500A are compatible with the company’s library of standard cells. (DI #2476)

To Vote For This Design, Circle No. 319

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**Circuit provides message on disabled phone line**

*Kevin Kelley, BAE Systems, Greenlawn, NY*

Phone companies often disconnect a misbehaving phone line from a complainant’s residence for troubleshooting purposes. With the problem between the residence and the central office, the residence is left with a dead phone line and no visible repairman while the line is under repair. The circuit in Figure 1 adapts a small key-chain voice recorder to the Tip and Ring lines of a phone line that has been disconnected from the central office. The purpose is to play a prerecorded message into any phone on the line when its receiver goes off-hook. A Radio Shack key-chain voice-memo recorder (part number 63-945) or a similar device provides solid-state voice-message storage and playback in a small package and also powers the phone line with its internal 6V batteries. You open and modify the recorder to bring four signals out to the external circuit: Battery (+), Battery (−), Speaker (+ or −), and the Play button contact. You can disconnect the internal speaker to save power.

With all phones on-hook, phone-line
Conventional shift registers, such as the 74HC595, require data-, clock-, and strobe-logic signals. The circuit in Figure 1 needs only two logic signals to isolate and control shift-register devices. For each transmitted bit and one of the two optocouplers receives a short drive pulse: one optocoupler for a high transmitted bit and the other for a low bit. After pulsing all the bits, the circuit a final concurrent 1 and 0 pulse strobes the data into the output registers. Two logic-gate packages on the isolated side of the circuit decode the two negative pulse signals back into data, clock, and strobe. Two NAND gates form an RS latch that captures the data state for the serial input (SERIN). Two more NAND gates form an AND to combine the two pulse sources into the SRCK shift clock. Finally, a NOR gate (or four more NAND gates) produces the RCK strobe. You can cascade the shift-register devices as necessary.

You have no timing constraints on the signals other than observing the maximum data rate of the optocouplers and ensuring an off period between pulses. The final latch pulse also generates an extra rising SRCK edge that you can use to load the first bit of the next sequence. In this case, the optocoupler that turns off last determines the RS latch state for the first bit. You can also ignore the extra clock; it has no effect on the output. Low power consumption is possible by keeping the pulses as short as possible by limiting the LED current and the updating rate. For example, with 40-μsec pulses and 1-msec period, the average drive current is 80 μA. (DI #2470)

To Vote For This Design, Circle No. 321

Optocoupler isolates shift registers
Jim Hartmann, Silent Knight LLC, Maple Grove, MN

Optocouplers allow you to isolate and control shift registers with only two logic signals.
Tack a log taper onto a digital potentiometer

Hank Zumbahlen, Analog Devices, Campbell, CA

It’s sometimes convenient to have digital control of the volume level in an audio system. The use of multiplying DACs (MDACs) is problematic because of the switching noise of the ladder network. This noise comes from the bit switches injecting charge into the signal when they turn on and off. Audio engineers have dubbed this noise “zipper noise” from the sound that results from dynamically adjusting the volume (gain riding). An alternative to an MDAC in this application is a digital potentiometer, such as the Analog Devices AD52XX, AD84XX, or AD7376. You can think of the digital potentiometer as a tapped resistor string. It generates less noise because fewer switches change state. In addition, you can connect the three terminals of the potentiometer anywhere within the common-mode range of the circuit (the supply-voltage range), unlike an MDAC, which generally uses ground as reference.

The primary drawback with using the digital potentiometer for volume control is that it currently comes with only a linear taper. With a linear taper, if the “wiper” is at the midpoint, the signal is only 6 dB less than the maximum. Thus, most of the adjustment range occurs within a small percentage of the range of the potentiometer. This constraint limits the adjustability of the volume setting. The ear responds logarithmically; the volume control should respond similarly. The primary reason for having only a linear taper is the manufacturing problems that the large range of resistance values for a log taper cause. By adding a pad resistor from the wiper of the potentiometer to one end (Figure 1a), you can simulate a log taper. If you split the potentiometer into two resistors, R1 and R2, you can redraw the circuit as in Figure 1b. The output voltage then depends on the parallel combination of R1 and Rpad.

You define a ratio, r, which is \( R_{\text{PAD}} / R_{\text{PAD}} \) (\( R_{\text{PAD}} = R_1 + R_2 \)). By adjusting the value of \( R_{\text{PAD}} \), you can modify r, which adjusts the taper, or the attenuation-versus-digital-input code to suit the application. The following expression gives the transfer function of the potentiometer:

\[
\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{R_2 R_{\text{PAD}}}{R_1 + R_2 R_{\text{PAD}}}
\]

Figure 2 shows the attenuation curves for three values of a pad resistor. As you can see, this trick doesn’t give a taper that is so many decibels per step, but it does allow for better low-level settable. You must address a couple of issues. The first is that the end-to-end resistance of the potentiometer changes with the digital code. It varies from the potentiometer resistance at one end (with the wiper at the lower end) to the value of the pad resistance in parallel with the potentiometer resistance at the other end. If you configure the circuit as a typical attenuator and drive it from a low-impedance source, the low pad resistance should not present a major problem. If, however, you are trying to obtain a set resistance value to determine a time constant (or any other application in which the resistor value is critical), this approach may not work well. The second issue involves overvoltage. The three terminals of the potentiometer can be anywhere within the supply range of the IC, which is 5V for the AD52XX and \( \pm 15V \) for the AD72XX family. If you apply overvoltage to one of the pins, even in a transient condition, the IC could latch up because of a parasitic substrate SCR. (DI #2473)
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