Feltier devices, also known as solid-state refrigerators, or TECs (thermoelectric coolers), actively cool temperature-sensitive electronic components, such as optical detectors and solid-state lasers. A glance at any TEC data sheet reveals that some primary and fairly easily understood parameters characterize a TEC: The maximum current is the TEC’s current drive for maximum cooling, the maximum differential temperature is the no-load cooling temperature at maximum current and with no heat load. The maximum voltage is the TEC’s voltage drop at the maximum-current drive, and the maximum heat transfer (Q_{\text{MAX}}) is the maximum cooling-heat load at a maximum current and differential temperature of zero.

However, one TEC data sheet proviso that designers sometimes miss is that you always measure these parameters with the TEC mounted on an effectively zero-thermal-impedance—that is, perfect—heat sink. This point is an important one and deserving of the designer’s rapt attention because heat sinks always have at least some thermal impedance, and all the primary TEC parameters change—sometimes dramatically—when the TEC must make do with an imperfect sink.

The family of impedance-versus-current curves in Figure 1 illustrates this effect. Each curve corresponds to a different heat-sink thermal impedance, normalized to one for 11 values from zero to two.

Although the maximum current is, by definition, the optimal current for...
maximum cooling at a heat-sink impedance of zero, the situation changes radically with increasing impedance until there's no net cooling whatsoever. Further, for impedance greater than one, instead of cooling, the maximum TEC drive actually heats rather than cools. Figure 2 shows the simple solution for this problem: You must replace the data sheet's maximum current and voltage values with new, lower maximum-drive values corresponding to the optimal numbers you need to achieve maximum cooling whenever impedance is greater than zero.

### Interface MIDI instruments to a PC through a USB port

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This Design Idea uses the FT232BM from Future Technology Devices International (www.ftdichip.com), a USB-to-UART interface IC that you need not program, to interface a USB port to the MIDI (musical-instrument-digital-interface) bus (Figure 1). The USB signals directly interface to IC1, an FT232BM. The serial-transmitter and -receiver signals pass through IC2 and IC3 to transform the RS-232 signals to the MIDI’s loop current. You can use an EEPROM, IC3, if you want to add a serial-number interface or use more than one interface.

This hardware doesn’t require you to write any software. However, you must install two drivers. First, you need the free VCP driver from FTDI at www.ftdichip.com/Drivers/VCP.htm. It allows you to use this interface as a common serial-port interface. Before you install it, you must change a string in the file FTDIPORT.INF (Reference 1) to set the 31,250-baud rate for FT232BM. Then, you can configure VCP to run at 38,400 baud. (The real baud rate will be 31,250 as preset in FTDIPORT.INI.)

Then, you must install another driver that permits you to see your VCP serial port as a MIDI port for addressing all MIDI messages. You can find a lot of similar drivers on the Internet. For example, the Roland serial MIDI driver is available at: http://www.roland.it/dow_drivers/for_win/serial32_wxp2k.exe. You can enable this driver on the COM1 or the COM3 port.

Listing 1, at www.edn.com/080417_NE21, shows the changes to add to the FTDIPORT.INF file that change the baud rate from 38,400 to 31,250 baud. Change this file before installation.

### Reference


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**Figure 1** This USB-to-MIDI interface uses the FT232BM, a USB-to-UART interface chip that you need not program.
Transmission lines simulate digital filters in PSpice

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Designers use PSpice mainly to simulate analog circuits. However, you can also simulate digital filters with it. The main components in a digital filter are delay elements, adders, and multipliers. Although you can implement adders and multipliers using operational amplifiers, you can simulate a delay element with a transmission line. The transmission line in PSpice is a long-forgotten element that can realize a delay of seconds.

For example, Figure 1 shows a second-order recursive digital filter. The transfer function for this filter is:

\[ H(z) = \frac{B_2z^2 + B_1z + B_0}{z^2 + A_1z + A_2}, \]

where \( H(z) \) is the digital-filter-transfer function, \( z \) is the \( z \)-transform variable, the \( A_n \) are the coefficients of the denominator polynomial of the transfer function, and the \( B_n \) are the coefficients of the numerator polynomial of the transfer function. You can obtain the coefficient values with software available for filter design (Reference 1). The sampling frequency, \( f_s \), relates to the transmission-line delay as \( t = \frac{1}{f_s} \). For example, a bandpass digital filter with a 3-dB passband from 900 Hz to 1 kHz, a sampling frequency of 6 kHz, and a Butterworth characteristic yields the following transfer function:

\[ H(z) = \frac{z^2 - 1}{z^2 - 0.90967072 + 0.809374}. \]

Figure 1 The transfer function for a second-order recursive digital filter has coefficient values that yield a lowpass, highpass, band-reject, or bandpass-transfer function.

In the PSpice circuit, the VCVSs (voltage-controlled voltage sources), E1 and E2, simulate voltage followers, and VCVSs E3 and E4 and the resistors that connect to them simulate summers.
In this case, the transmission-line delay is $1/6000 = 166.67 \ \mu s$. If you additionally specify an impedance, $Z$, of 1\Omega for the transmission line, then the parameters for the transmission line are $Z_p = 1\Omega$, and $t = 166.67 \ \mu s$. Figure 2 shows the PSpice circuit. The VCVSs (voltage-controlled voltage sources), E1 and E2, simulate voltage followers, and VCVSs E3 and E4 and the resistors that connect to them simulate summers. Figure 3 shows the results of the simulation.

**REFERENCE**


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### Dual flip-flop forms simple delayed-pulse generator

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Some applications require clock-timing adjustments, such as generating precision clocks for time-interleaved ADCs, or delay adjustments in a variety of precision-timing and pulse-delay applications. This Design Idea describes a delayed-pulse generator using a dual-CMOS D-type flip-flop (Figure 1). The circuit provides precision time delays of a trigger input pulse. A dc-control voltage selects a time delay within the full-scale range. When the rising edge of a pulse triggers the input, the circuit’s output generates a pulse with its rising edge delayed by an amount equal to the selected time delay, $T_{PD}$, plus a fixed inherent propagation delay $T_{PD}$. Also, a time constant, $R_C$, determines the output pulse’s width.

A precision dc source, $I_{th}$, and capacitor $C_{th}$ set the full-scale delay range. When $Q_1$ is off, the current source charges capacitor $C_{th}$, generating a linear-ramp voltage with slope equal to $I_{th}/C_{th}$. The delay is the time it takes for the ramp to rise from its initial voltage to the control-voltage value.

In this application, the ramp slope is 10 mV/1 \mu s, so that the full-scale delay range is 256 \mu s for a control voltage of 0 to 2.56V. You can set the full-scale delay by changing $L_{th}$ through either $R_3$ or capacitor $C_{th}$. For best accuracy, the current source can range from 10 \mu A to 1 mA, the capacitor’s value can range from 1 nF to 1 \mu F, and the corresponding full-scale delay can range from 2.56 \mu s to 256 msec. Use a precision film capacitor for $C_{th}$.

The basis of the current source is a shunt precision-micropower-voltage-reference, $I_{th}$, producing a reference voltage of 1.233V with an initial ac...
accuracy of 0.2%. A Texas Instruments (www.ti.com) LM4041, through precision resistors R₁ and R₂, biases the Darlington-coupled transistors Q₁ and Q₂ with a reference current $I_0 = \frac{V_{\text{REF}}}{R_1 + R_2} = 100 \, \mu A$. The Darlington configuration ensures that base current is negligible and that the output collector current can achieve a worst-case accuracy of 0.3%. You can use any small-signal transistor, but, for best accuracy, use high-gain, low-level, low-noise BJTs, (bipolar-junction transistors) such as a 2N5087 or a BC557C.

IC₁ₐ is a one-shot circuit (Reference 1). The output pulse's width, $T_w$, is $R_4C_2 \ln(V_{\text{DD}}/V_{\text{TH}})$, where $V_{\text{TH}}$ is the threshold voltage of the digital CMOS. Because $V_{\text{TH}} \approx V_{\text{DD}}/2$, then $T_w \approx R_4C_2 \times 0.69$. Diode D₁ reduces recovery time. After power-up, Q₁ is in saturation, absorbing the current source’s output, and, as soon as an input pulse triggers the circuit, IC₁ₐ’s Q output goes low, switching off Q₂, starting a ramp. When the ramp exceeds the control voltage, then the IC₂ₐ comparator’s output goes high, and the rising edge triggers one-shot IC₁₈ and switches on Q₃ through IC₁₈’, allowing the discharge of the capacitor C₁. When an input pulse triggers the circuit, any other trigger pulse that occurs before the falling edge of the delayed output pulse does not produce an output pulse; in other words, the circuit is not retriggerable. This feature permits you, at the same time, to divide and delay an input-trigger clock.

Although IC₁ and IC₂ can operate from a 3 to 16V supply, the minimum supply voltage of the circuit is 5V; otherwise, Q₁ and Q₂ approach saturation. Voltage comparator IC₂₈, an STMicroelectronics (www.st.com) TS3702, has an input-common-mode-voltage range that includes ground, permitting you to monitor input voltages as low as 0V.

However, for correct operation of the circuit, the minimum control voltage must be greater than the saturation voltage of Q₁. For the components in Figure 1, the measured value is 12 mV. If you want to reduce this voltage, you can use a digital N-channel MOSFET with low on-resistance. The optional input lowpass filter, comprising R₆ and C₄, helps to clean noise from the dc-control voltage.

If a DAC drives the control input, you can build a digitally programmable delay generator. A suitable low-cost, 8-bit DAC is the AD558 from Analog Devices (www.analog.com), which features an internal precision bandgap reference to provide an output voltage of 0 to 2.56V, making 1 LSB equal to 1 µsec. It operates from 5 to 16V, with a 1-µsec settling time. The circuit’s quiescent current, $I_{\text{Q0}}$, is less than 300 µA because all ICs are micropower.

REFERENCE